APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER M. TECH DEGREE EXAMINATION

Electronics & Communication Engineering

(VLSI and Embedded Systems)

04EC7509—HIGH SPEED DIGITAL DESIGN

Max. Marks : 60 Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. Explain lumped and distributed system with suitable example.
2. Examine the self inductance of probe ground loops.
3. Demonstrate EMI and crosstalk of point to point wiring.
4. Derive the characteristic impedance of an ideal transmission line at high speeds.
5. Comment on the capacitance offered by vias.
6. Illustrate end termination with suitable figures.
7. Sketch and explain the timing analysis showing clock skew.
8. What is delay adjustment? List different types of delays.

PART B

Each question carries 6 marks

9. Express the effect of sudden change in the current and voltage in the speed of operation of logic circuits.

OR

10. List the reasons for power dissipation in a digital circuit with an example.

11. Illustrate rise time and bandwidth of oscilloscope with necessary expressions and figures.

OR

12. With the help of electrical model of oscilloscope, explain the process involved in the estimation of self-inductance of probe ground loop and Q value of the probing circuit.

13. Demonstrate Timing Margin and its relation to Clock Skew.

OR

14. With necessary equations, explain the problem of point to point wiring at high frequencies.

15. Interpret lossless transmission lines at high speeds with necessary equations.

OR

16. Explain Skin effect and its mechanics at very high speeds.

17. Summarize DC biasing of end termination.

OR

18. Illustrate the mechanical properties of Vias

19. With suitable diagrams, briefly discuss the design rules to be followed for providing stable voltage reference to the digital systems.

OR

20. What is “Clock Jitter”? Give the reasons for the same. Discuss different methods for avoiding clock jitter.