



APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
THIRD SEMESTER M.TECH DEGREE EXAMINATION
Electronics & Communication Engineering
(VLSI and Embedded Systems)
04EC7503—System on Chip

Max. Marks: 60

Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. List the key points to SoC design process.
2. Write the significance of communication centric design flow in SoC.
3. Describe the major benefits of cache architecture in memory design of MPSoC.
4. Show the expression for execution path timing analysis of MPSoC.
5. List the limitation of SoC over NoC.
6. Comment on *arbitration* among NoC and SoC.
7. List the types of network topologies in NoC.
8. Explain QoS in NoC and list the categories of QoS.

PART B

Each question carries 6 marks

9. Write short notes on SoC and its design flow.
OR
10. Discuss HW-SW co-design process of SoC.
OR
11. Write in detail about different types of arbitration schemes in SoC.
OR
12. Illustrate the principles of AMBA bus architecture in detail.
OR
13. With neat diagram, explain the energy aware memory design of MPSoC.
OR
14. Explain in detail about energy aware processor design in MPSoC.
OR
15. Show the modeling of shared resources in MPSoC.
OR
16. With neat diagram, illustrate the architecture component modeling and analysis of MPSoC.
OR
17. With neat diagram, explain ASIC to system and NoC.
OR
18. Write the comparison between NoC based and bus based system design.
OR
19. Describe switching strategies in NoC and explain its types in detail.
OR
20. With neat diagram, explain the principle and types of flow control schemes in NoC.