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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2017

Course Code: AE363

Course Name: VLSI CIRCUIT DESIGN (AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1	a)	Explain CMOS IC technology fabrication steps with neat figures.	(8)
	b)	Explain the switching operation of an enhancement type N- MOFET and draw the transfer characteristics of it.	(7)
2	a)	Explain drain induced barrier lowering and velocity saturation in MOSFETs.	(8)
	b)	Compare of CMOS, Bipolar and GaAs technology.	(7)
3	a)	Explain the procedure of implanting the ions into the silicon wafer with a neat figure.	(7)
	b)	Explain cut off, linear and saturation modes of operation of an enhancement type N- MOSFET with necessary equations.	(6)
	c)	Draw the drain characteristics of enhancement type N-MOSFET.	(2)

PART B

Answer any two full questions, each carries 15 marks.

4	a)	Explain the operation of two input NAND gate using CMOS logic with its circuit diagram and truth table.	(7)
	b)	Draw the layout of a two input NOR gate.	(8)
5	a)	Explain a two input NOR gate using pseudo NMOS logic with its circuit diagram and truth table.	(8)
	b)	What are the uses of stick diagrams in layout?	(2)
	c)	Draw the stick diagram of a two input NAND gate.	(5)
6	a)	Draw the circuit diagram of three inputs AND gate using domino logic and explain its operation.	(8)
	b)	Draw the stick diagram of a two input NOR gate and explain about each different layer.	(7)

PART C

Answer any two full questions, each carries 20 marks.

7	a)	Explain constant voltage scaling and its effect on device parameters.	(10)
	b)	Explain the impact of skew and jitter in VLSI system with a neat figure.	(10)
8	a)	Explain constant electric field scaling and its influence on different device parameters.	(10)
	b)	Explain the timing classifications in digital systems.	(10)
9	a)	Explain three basic arrangements for the bus lines.	(10)
	b)	Explain about slack borrowing technique in latch based clocking.	(10)

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