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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

**FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2017**

**Electronics & Communication Engineering**

**(VLSI and Embedded Systems)**

## 04EC6505—CMOS VLSI Design

Max. Marks : 60 Duration: 3 Hours

**PART A**

***Answer All Questions***

***Each question carries 3 marks***

1. Explain about noise margin?
2. Explain the impact of crosstalk?
3. Realize three input NOR gate with static CMOS logic? Explain the operation.
4. Explain negative edge triggered master slave D flip-flop using CMOS logic?
5. Explain two input XOR/XNOR gate using DCVS logic?
6. Explain two input pseudo NMOS NOR gate?
7. Explain zipper CMOS circuits?
8. Explain the operation of TSPC based rising edge triggered D flip-flop?

**PART B**

***Each question carries 6 marks***

9. Explain CMOS inverter circuit along with its VTC characteristics? Derive the expressions for Noise margin?

OR

10. Design and explain the working of tristate inverter? Explain the working of depletion load and enhancement load inverters?
11. Explain logical effort of two input NAND and NOR gate? Derive the general expression for N input NOR and NAND gate?

OR

12. Explain about finding out the delay in a multistage logic network?
13. Realize the Boolean expression $Z= \overline{PQ+ (R+S) T}$ using static CMOS as well as using depletion type MOSFET as load?

OR

14. Explain the implementations of AOI and OAI gates using CMOS logic with an example?

15. Implement and explain the operation of D latch using CMOS implementation with necessary waveforms?

OR

16. Implement and explain the operation of CMOS SR latch using NOR gates with its truth table?
17. Implement OR/NOR, AND/NAND and XOR/XNOR using Complimentary pass transistor logic?

OR

18. Explain the working of two input AND gate using pass transistor logic? Explain the requirement of level restorer circuit in pass transistor logic?
19. Explain two different types of NORA CMOS logic with its circuit diagram and operation?

OR

20. Explain ratioed and ratioless enhancement load dynamic shift register?