F 3151 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering/Information Technology

CS 010 305/IT 010 304—SWITCHING THEORY AND LOGIC DESIGN (CS, IT)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 3 *marks.*

1. Find the value of x in the following :—

   (a) $(847)_{10} = (x)_{16}$.

   (b) $(10110101)_2 = (x)_8$.

   (c) $(A3BH)_{16} = (2619)_{10}$.

2. Draw a half adder circuit using NOR gates only.
3. Write down the truth table and characteristic equation of SR flip-flop.
4. How are shift-left or shift-right transfer registers built ?
5. What do you mean by hazard-free asynchronous sequential circuits ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Convert the following into cannonical forms :

   (a) $\overline{A}B + AB\overline{C}D + \overline{B}\,\overline{C}$.

   (b) $(\overline{A} + C)(A + \overline{B})(B + C)$.

7. Using full-adder blocks, represent the following 4-bit addition :

   1111 + 1011.

Turn over

8. Distinguish between truth table and excitation table, taking JK flip-flop as example. How the excitation table can be derived from the truth table ?

9. Construct a Johnson counter for ten timing signals ?

10. What is fault tolerance ? Explain different fault tolerance techniques.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Design the circuit for a 2 bit BCD-to- binary coverter, with the help of the function tables.

Or

12. Reduce using Quine McCluskey method $S = \sum (1, 2, 4, 5, 6, 8, 9, 12) + d\,(3, 10, 13, 15)$. Draw reduced prime implicants table and the minimal reduced circuit.

13. (a) What is a full subtractor ? Design the same using K-maps and draw the minimal circuit. (6 marks)

(b) With a neat block diagram, explain a 4 bit carry look-ahead adder. (6 marks)

Or

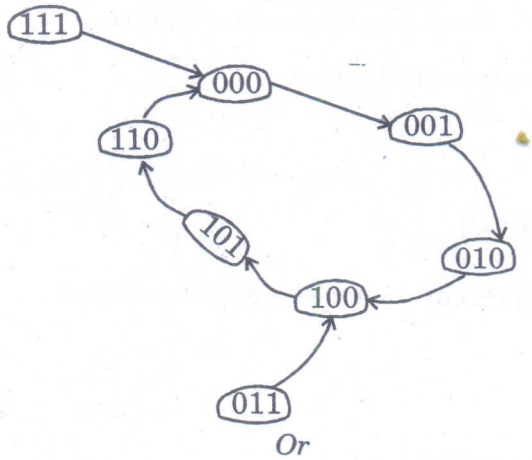
14. Design a gray-to-binary code converter using 4 : 1 MUX. Draw the circuit diagram and explain.

15. A network produces a '1' output if and only if the current input and the previous three inputs correspond to either of the sequences 0110 or 1001. The output '1' is to occur at the time of the fourth input of the recognised sequence. Outputs of zero are to be produced at all other time. Construct the state diagram.

Or

16. Design a sequential machine with one input and one output line such that the output becomes '1' when the input receives a sequence 101. Overlapping of sequence is allowed. Use D-flip-flops.

17. Design a synchronous counter using JK flip-flop for the state diagram given in figure.



Or

18. (a) With neat diagrams and waveforms, explain a 4 bit shift register with left/right shift control and with parallel load control.

(6 marks)

(b) Design a mod-77 synchronous counter by cascading two 4-bit binary counters. (6 marks)

19. (a) With an example, explain one method of designing a hazard-free network. (5 marks)

(b) Design the following network, which is free of static and dynamic hazards. Design the circuit using NAND gates only $F(a, b, c, d) = \sum m(1, 5, 7, 14, 15)$.

(7 marks)

Or

20. (a) Draw the internal circuit diagram of a CMOS NAND gate and explain its working.

(7 marks)

(b) Compare the performance parameters of TTL, CMOS and ECL families. (5 marks)

(5 × 12 = 60 marks)