APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER M.TECH DEGREE EXAMINATION

Electronics & Communication Engineering

(VLSI and Embedded Systems)

04EC7503—System on Chip

Max. Marks: 60 Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. List the key points to SoC design process.
2. Explain the elements of bus based on chip communication architecture.
3. Write the importance of gating supply rails in energy aware processor design of MPSoC.
4. List the platform design challenges in MPSoC.
5. Describe the principle of NoC with neat diagram.
6. Write the limitation of SoC over NoC.
7. Explain the significance of routing algorithm in NoC.
8. Explain the types of clocking schemes in NoC.

PART B

Each question carries 6 marks

9. Discuss SoC spiral model with neat diagram

OR

10. Illustrate how HW-SW co-design process in SoC differs from classic HW-SW design process.

11. With neat diagram, explain the types of bus topologies in SoC.

OR

12. Write in detail about different types of arbitration schemes in SoC.

13. Illustrate the principle of energy ware processor design in MPSoC.

OR

14. Explain in detail about energy aware on chip communication system design in MPSoC.

15. Discuss the role of performance modeling in MPSoC.

OR

16. Write short notes on architecture and global analysis of MPSoC.

17. Write the comparison between bus based and NoC based system design.

OR

18. Write short notes in NoC with neat diagram.

19. With neat diagram, explain the principle and types of flow control schemes in NoC

OR

20. Explain the principles of routing algorithm and its types in deatil.