APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER M.TECH DEGREE EXAMINATION,

Electronics & Communication Engineering (VLSI and Embedded Systems)

04EC7509—HIGH SPEED DIGITAL DESIGN

Max. Marks: 60 Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. Differentiate between lumped and distributed system with an example.
2. An oscilloscope rated at 300 MHz was purchased and its probe was also rated at 300 MHz. Both specifications are 3 dB bandwidths. How will this combination affect the rise time of the signal displayed when the input signal has 2ns rise time?
3. Why does point- to-point wiring generate EMI?
4. Derive the characteristic impedance of an ideal transmission line at high speeds.
5. Comment on the capacitance offered by vias.
6. Illustrate end termination.
7. Sketch the timing analysis showing clock skew and explain.
8. What is delay adjustment? List the different types of delays.

PART B

Each question carries 6 marks

9. Discuss the effect of sudden change in the current and voltage in the speed of operation of logic circuits.

OR

10. What are the reasons for power dissipation in a digital circuit? Explain each type.

11. Explain rise time and bandwidth of oscilloscope with necessary expressions and figures.

OR

12. With the help of electrical model of oscilloscope, explain the process involved in the estimation of self-inductance of probe ground loop and Q value of the probing circuit.
13. Discuss the problems of signal distortion and cross talk in point-to-point wiring at high frequencies with necessary equations.

OR

14. Explain how slowing down of a clock system affects the overall performance of a high speed digital system with special reference to metastability in clock distribution.
15. Compare and contrast the features of low – loss and lossy transmission lines. State the unique properties of lossless transmission lines.

OR

16. Explain Skin effect and its mechanics at very high speeds.
17. Summarize end terminations in the following respects (a) Rise time by intuition and calculation (b) DC Biasing.

OR

18. Illustrate the mechanical properties of vias
19. With suitable diagrams, briefly discuss the design rules to be followed for providing stable voltage reference to the digital systems.

OR

20. Explain the significance of timing margin at high speeds. What is Clock Jitter?