APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION
ELECTRONICS& COMMUNICATION ENGINEERING
(VLSI & EMBEDDED SYSTEMS)
04EC6505 - CMOS VLSI DESIGN

Time: 3 hrs Max. Marks: 60

PART A

(Answer all questions. Each question carry 3 marks).

1. Define a. Switching power dissipation b. Short circuit power dissipation (3)
2. What is meant by logical effort and parasitic delay of a circuit? (3)
3. Realize the expression $Z = \overline{A + BC(D + E)}$ using NMOS depletion-load complex logic gate. (3)
4. Draw the circuit diagram of a CMOS SR latch circuit based on NOR2 gate. (3)
5. What are the advantages of transmission gate? (3)
6. List various static logic circuit style. (3)
7. Define voltage bootstrapping in dynamic logic style. (3)
8. What is charge sharing problem in domino logic? (3)

PART B

(Each full question carries 6 marks).

9. With a relevant VTC curve explain the static characteristics of a CMOS inverter (6)

OR

10. What are the sources of power dissipation in a CMOS inverter?. Derive the expression for dynamic power dissipation. (6)
11. What is meant by logical effort? Discuss the logical effort of a 3 input NOR gate. (6)

OR

12. Draw the RC delay model of a CMOS inverter. Derive the expression for fall and rise delay time (6)
13. Briefly analyze the static characteristic of a 2 input NOR gate with NMOS load (6)

OR

14. Draw the CMOS implementation of $Y = \overline{(A + B + C)(D + E)}$. Assuming that for all input $(\frac{W}{L})_p$ =15, for all PMOS transistors and $(\frac{W}{L})_n$ =10 for all NMOS transistors. Find the Equivalent CMOS inverter size. (6)
15. Analyze the operation of a RS latch using CMOS with necessary timing diagram. (6)

OR

16. Explain the behaviour of a bistable element with suitable diagram. (6)

17. Implement a 3 input XOR functions using each of the following circuit techniques (6)

    a. Static CMOS b.Pseudo-nMOS

OR

18. Analyze the Pass Transistor logic with its advantages and disadvantages. (6)

19. Illustrate the working of domino CMOS logic gate with necessary diagram. (6)

OR

20. Explain the basic principle of voltage boot strapping with suitable diagram. (6)