APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION

Electronics & Communication Engineering

(VLSI and Embedded Systems)

04EC6503—ADVANCED DIGITAL DESIGN

Max. Marks : 60 Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. Illustrate Shannon's expansion theorem . .
2. Explain critical and non critical race with examples
3. Design a 4-bit up counter with parallel load.
4. Compare horizontal and vertical microinstruction
5. Explain the steps for RTL Design.
6. Explain the conversion of C code to high level state machine with an example.
7. Explain the significance of operator binding and operator scheduling while designing a circuit
8. Differentiate optimization and trade off.

PART B

Each question carries 6 marks

9. Design a Moore FSM to detect the occurrence of the sequence 1100

OR

10. Write down the HDL code for a) 4 bit Ripple Carry Adder and b) 4 bit Carry Look Ahead Adder

11. Discuss about static and dynamic hazards. Also explain about the elimination of hazards .

OR

12. Draw the ASM chart for a binary multiplier

13. Design a 4 bit magnitude comparator.

OR

14. Design a 4 bit register with maintain the present value, shift right, shift left, load and clear functions.
15. Design a controller for soda dispenser processor.

OR

16. Illustrate the working of micro programmed controller with neat diagram
17. Design a laser based measurement system using RTL design method.

OR

18. IIllustrate the significance of critical path delay in determining the clock frequency of a circuit.
19. Design a 4 bit sequential multiplier (shift and add style) .

OR

20. Explain different state encoding methods.