

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SECOND SEMESTER M.C.A. DEGREE EXAMINATION, DEC 2018

Course Code: RLMCA112

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE

Max. Marks: 60

Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks.

Marks

- | | | |
|---|---|-----|
| 1 | Distinguish between Big-endian and Little endian byte addressable memory. | (3) |
| 2 | Explain auto increment and auto decrement addressing modes. | (3) |
| 3 | What is WMFC? What is role of WMFC in memory read and write? | (3) |
| 4 | Explain multiple bus Organization, with a diagram. | (3) |
| 5 | Explain memory mapped I/O and I/O mapped I/O, | (3) |
| 6 | Explain the operation of SRAM cell | (3) |
| 7 | Write a note on memory operations : a)write back b)write through | (3) |
| 8 | What is memory interleaving? | (3) |

PART B

Answer any one question from each module. Each question carries 6 marks.

Module I

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|---|---|-----|
| 9 | With the help of a neat block diagram, describe the basic functional units of a computer. | (6) |
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OR

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| 10 | Explain different basic instruction types with examples. | (6) |
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Module II

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| 11 | Discuss any 4 different addressing modes. | (6) |
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OR

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| 12 | What do you mean by a subroutine? Also explain subroutine nesting with the help of a processor stack. | (6) |
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Module III

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| 13 | Explain the execution of a complete instruction with an example | (6) |
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OR

14 With neat diagrams, explain hardwired and microprogrammed control units. (6)

Module IV

15 What is DMA? Explain the different modes of operation. (6)

OR

16 Explain how pipelining can improve the speed of processing with necessary diagram. (6)

Module V

17 Explain about different types of ROM. (6)

OR

18 With a neat diagram, explain Synchronous DRAM. (6)

Module VI

19 Explain different cache - memory mapping functions. (6)

OR

20 How the virtual address is converted into real address in a paged virtual memory system? Explain. (6)
