B

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SECOND SEMESTER M.TECH DEGREE EXAMINATION MAY/JUNE 2016
(2015 Admissions)
ELECTRONICS & COMMUNICATION ENGINEERING
VLSI & Embedded Systems
04 EC 6504: ADVANCED CMOS VLSI

Time: 3 hrs Max. Marks: 60

PART A
(Answer all questions. Each question carry 3 marks).

1. Draw and explain the MIS structure (with p-type semiconductor) under strong inversion condition. What is meant by threshold voltage? (3)
2. Discuss the various side-effects of low-voltage design. (3)
3. Draw the circuit diagram of a 3-input NAND gate in static CMOS and pseudo-NMOS logic. (3)
4. Show the implementation of XOR/XNOR gates using CPL. (3)
5. Implement the function $Z = AB + (C + D)(E + F) + GH$ using Domino CMOS logic. (3)
6. What are the salient features of domino logic family? (3)
7. Illustrate the basic features of SRAM using a generic RAM organization. (3)
8. Explain how the use of a 'dummy column' in the RAM tailors the width of pulsed wordline to the access time of RAM? (3)

PART B
(Each full question carries 6 marks).

9. Write a short note on the various leakage mechanisms in deep submicron transistors. (6)

OR

10. Discuss different sources of power dissipation in CMOS. (6)
11. Briefly explain the various runtime active leakage reduction techniques in logic with suitable diagrams. (6)

OR

12. How do the design time techniques reduce leakage in logic? Explain with suitable diagrams. (6)
13. Discuss the various multiple-threshold techniques to achieve low leakage under performance constraint. (6)

OR

14. Explain various submicron device design issues and what are the difficulties for low-power and low-voltage operation? (6)

15. Show how the function $x_1x_2 + x_2x_3 + x_3x_1$ can be realized using a DCVS logic using suitable diagrams. (6)

OR

16. Explain a 1.5V BiCMOS buffer circuit with transient feedback with the help of a neat diagram. (6)

17. Draw the circuit diagram of NORA CMOS logic and explain with an example. How is the Precharge/Evaluation phases scheduled in NORA logic? (6)

OR

18. Draw and explain the circuit topology of precharged high DCSL. (6)

19. Draw a 6T SRAM cell and explain how the read and write operation takes place in the cell. (6)

OR

20. What are the various low-voltage low-power SRAM cell designs? (6)