APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Scheme for Valuation/Answer Key

Scheme of evaluation (marks in brackets) and answers of problems/key

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION (S), MAY 2019

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

		Marks
1	CPU time-definition - 1 mark formula-1 mark Throughput-definition – 1 mark formula-1 mark	(4)
2	Numa model illustration-2 marks explanation – 2 marks	(4)
3	Spatial locality-2marks Temporal locality-2marks	(4)
4	Generalized model of multiprocessor- 2 marks Explanation- 2marks	(4)
5	Write-invalidate with diagram -2 marks Write-update with diagram -2 marks	(4)
6	Speedup-2 marks Efficiency-1 mark Throughput-1 mark	(4)
7	Internal forwarding example with diagram- 4 marks	(4)
8	CSA with example- 2 marks CPA with example -2 marks	(4)
9	Distributed caching explanation-4 marks	(4)
10	SCI interconnect model diagram- 2 marks Explanation- 2 marks	

PART B

Answer any two full questions, each carries 9 marks.

11	a)	Bernstein's conditions- 2 marks Significance – 2marks	(4)
	b)	Parallel instructions identification using Bernstein's conditions-5 marks	(5)
12	a)	Memory hierarchy diagram+explanation-3 marks	(3)
	b)	average access time -2.5 marks	(6)

average byte cost-2.5 marks

13 a) SIMD operational model (5-tuple)+explanation-3 marks (3)

b) Superscalar architecture- 3 marks (6)

Superscalar pipelining+diagram- 3 marks

PART C

Answer any two full questions, each carries 9 marks.

14 a) Hot spot problem explanation- 3 marks (3)

b) Network Design-2 marks (6)

Routing- 3 marks

Blocking and non-blocking – 1 marks

15 a) Linear pipeline with diagram-1.5 marks (3)

Non –linear pipeline with diagram-1.5 marks

b) Forbidden latencies - 1mark (6)

Transition diagram - 2marks

Simple and Greedy cycles - 1 mark

MAL - 1 mark

Throughput - 1mark

16 a) Write- invalidate snoopy protocol transition diagram with explanation-4 marks (4)

b) Store-and –forward-2.5 marks (5)

Wormhole routing-2.5 marks

PART D

Answer any two full questions, each carries 12 marks.

17 a) Effect of branching-2 marks (9)

Two branch handling techniques-7 marks

b) Scoreboarding explanation- 3 marks (3)

18 a) Multicontext processor model +explanation- 6 marks (6)

b) Problems of asynchrony-2 marks (6)

Solutions-4 marks

19 a) Design and performance of superpipelined processor- 3 marks (6)

Design and performance of superscalar superpipelined processor- 3 marks

b) Architecture-3 marks (6)

Explanation 3 marks

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