Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks Marks

1		Convert AD_{16} to its equivalent decimal and binary form.	(5)
2		Express $F = \Pi M(1,5,7)$ using SOPs and POSs and minimize the expression.	(5)
3		What is meant by race around condition? How can it be avoided?	(5)
4		Realise a full adder using the 3x8 decoder.	(5)
5		Explain Johnsons ring counter with an example.	(5)
6		What is the difference between a Moore and Mealy machines? Explain with examples?	(5)
7		Explain the working of a three-bit R-2R ladder DAC.	(5)
8		Implement $F = \Sigma m(2,3,4,5,7)$using PAL.	(5)

PART B

Answer any two questions, each carries 10 marks

9	a)	Determine the range of numbers that can be represented using signed bit, 1's complement and 2's complement form for a word length of 8 bits. Also represent and using word length of 8 bit in signed bit, 1's complement and 2's complement form.	(5)
	b)	Digital data is to be transmitted with even parity for transmitting the letter A in ASCII code. Discuss how is parity added to digital data to detect errors in transmission?	(5)
10	a)	Draw and explain the operation of TTL NAND gate.	(5)
	b)	Simplify the Boolean expression using K-map and draw the logic diagram. $F(A,B,C,D) = \sum m(0,1,5,12,13,15) + d(1,3,56)$	(5)
11	a)	Convert gray code to binary and hexadecimal.	(3)
	b)	Minimize the Boolean expression F=AB'C'+C'D+BD'+A'C using K -map and implement the logic circuit using NAND gates only.	(7)

PART C

Answer any two questions, each carries 10 marks

12 a) Realise the Boolean expression $F = \Sigma m(1,5,7,15)$ using a 4 x 1 Multiplexer (5)

b) Realise a full adder using two half adders. (5)

13 a) Discuss the different types of shift registers. (5)

b) Design a 3 bit asynchronous counter using JK flip flops. (5)

14 a) What is a glitch? Show the timing diagram for a Mod 6 asynchronous counter showing the glitches in the diagram. (5)

b) How can a 2:4 decoder be used as 1:4 Demultiplexer? (5)

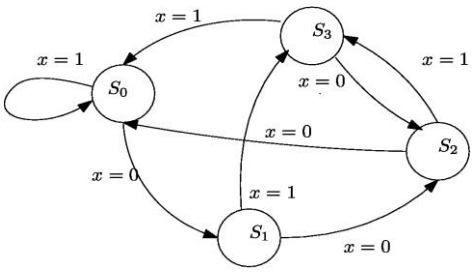
PART D

Answer any two questions, each carries 10 marks

15 a) Develop the logic circuit diagram and table for 4 -bit ring counter and explain the working. (5)

b) Explain the working of Flash type ADC. (5)

16 Develop the state diagram and design the sequential circuit using T flip flops. Also, draw the logic circuit diagram. (10)



$S_0 = 101, S_1 = 111$

$S_2 = 110, S_3 = 011$

17 a) Bring out the differences between a PAL and PLA. (4)

b) Write a VHDL program for a Full Adder (use structural approach). (6)

****