Course Code: CS203

Course Name: SWITHCING THEORY AND LOGIC DESIGN

Max. Marks: 100 | Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks.

			Marks
1		Any *three* advantages of digital systems over analogue systems- 1 mark each	(3)
2		Each conbversion- i)1266(1.5 marks) ii)01100111 (1.5 marks).	(3)
3		K-map contents- 1.5 mark each	(3)
4		Complement of A+BC′(D+EF′)′- 3 marks	(3)

PART B

Answer any two full questions, each carries9 marks.

5	a)	(i) *1's complement* of the binary number1101.01- 0010.10 -2 marks. (ii) Compute *8's complement* of the octal number 672.23-105.55 - 2 marks. (iii) Ans: 10EF Addition -3 marks.	(7)
	b)	Decimal number 6.25 in binary- 2 marks 6.25=110.01= 1.1001 x 2^2 Sign bit=1 Exponent – 000010 Mantissa-100100000	(2)
6		Tabulation-5 marks Prime Implicants- 1 mark Essential Prime Implicant- x′z +x z′ 2 marks Simplified Expression- 1 mark. Ans x′z+ xz′	(9)
7	a)	i)*canonical PoS*- π(0,4)-2.5 marks ii) *standard PoS*- (x+z)(x+y) 2.5 marks	(5)
	b)	Subtraction using *10's complement* addition- 4 marks Ans -834	(4)

PART C

		Answer all questions, each carries3 marks.	
8		*master-slave J-K flip-flop* realized using NOR and AND gates- 3 marks	(3)
9		truth table of a 4x1 de-multiplexer -1.5 marks logic diagram- 1.5 marks.	(3)
10		*full-subtractor* design – 2 marks implementation using a decoder and 1 OR gate – 1 mark	(3)
11		*half-adder* expression- 1 mark Diagram using NAND gates- 2 marks	(3)
		PART D	
		Answer any two full questions, each carries 9 marks.	
12	a)	Boolean functions using a 2X1 multiplexer and additional gates – 3 marks Any valid design can be given marks. (For eg using 2 2x 1 MUX with enable input , implementing 4 x 1 MUX with 2 x 1 MUX etc)	(3)
	b)	Truth table- 1 mark Code converter simplification using K-map- 3 marks Le inputs be ABC outputs be C1C2 C3 C1= AC′ +AB′ +A′BC C2=B′C + B C′ C3=B′C′ + B C′ Diagram- 2 marks	(6)
13	a)	Consider the ouputs of 2-bit subtractor Difference and Borrow . If they are equal comparator output for =1 . If difference < borrow Comparator output for <= 1 else comparator output for > = 1.Write the truth table – 1 mark. K-map design 2 marks.	(3)
	b)	State table – 1 mark Simplification using K-map- 3 marks Diagram- 2 marks Inputs are A, B,x. Using K – Map TA= A′x+Bx+AB′x′ TB= (A XOR B)x +A′B′x′	(6)
14		*state table* – 6 marks st*ate diagram* – 3 marks	(9)
		PART E	
		Answer any four full questions, each carries10 marks.	
15		Diagram- 5 marks Working of serial adder- 5 marks.	(10)
16		State table – 1 marks Simplification using K-map- 6 marks J2 = Q0' , K2 = Q1' ; J1 = Q2' , K1 = Q2Q0 ; J0 = Q2 , K0 = Q1Q2' Diagram- 3 marks	(10)
17		*mod-16 ripple up-counter* using J-Kflip-flops.- 4 marks *mod-12 ripple counter- 6 marks. In mod 12 Q3Q2 output should be connected to NAND gate. Output of NAND gate comnnected to Clear input.*	(10)
18	a)	Any 3 differences- 1 mark each	(3)
	b)	*read-only memory* and *read-write memory*- 2 marks each	(4)
	c)	Fig represents mod 2 ripple counter. Its timing diagram- Q1-1.5 marks Q2-1.5 marks	(3)
19	a)	PLA- 4 marks	(4)
	b)	Simplification using K-map – 2 marks each Diagram- 2 marks	(6)
20		Algorithms / Flowchart for *floating point addition* – 5 marks *floating point subtraction* – 5 marks	(10)

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2019