APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Scheme of Valuation/Answer Key

Scheme of evaluation (marks in brackets) and answers of problems/key

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

		Marks
1	Architecture - 2 marks Explanation - 2 marks	(4)
2	Flow chart - 2marks Explanation - 2 marks	(4)
3	Any four differences - 4 marks	(4)
4	Cross bar network - explanation - 2 marks Multiport memory - explanation - 2 marks	(4)
5	Process migration - example with diagram - 2 marks I/O - example with diagram - 2marks	(4)
6	Store and forward routing – explanation - 2 marks Wormhole routing - explanation - 2 marks	(4)
7	Three hazards- with example - 4 marks	(4)
8	τ = 9 ns frequency =1/τ =111.11 MHz	(4)
9	Static dataflow computers - 2marks Dynamic dataflow computers - 2marks	(4)
10	Four policies - 4 marks	(4)

PART B

Answer any two full questions, each carries 9 marks.

11 a) Four classes with diagram - 4 marks (4)

b) Average CPI = $\frac{35000\times1+20000\times2+15000\times2+6000\times2}{35000+20000+15000+6000}$ (5)

= 1.54 cycles/instruction ---------- 2 marks

MIPS = $\frac{f}{CPI\times10^6}$ = $\frac{40\times10^6}{1.54\times10^6} = 25.97MIPS$ --- 2 marks

Execution Time - $\frac{I_c\times CPI}{f} = \frac{(35000+20000+15000+6000)\times1.54}{40\times10^6} = 2.93msec$--1 mark

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T=$\frac{I_c}{MIPS\times10^6}=\frac{35000+20000+15000+6000}{25.97\times10^6}$=2.93 msec

12 a) Hit Ratio - Definition +formula - 1.5 marks (3)

Effective access time – Definition + formula - 1.5 marks

b) =h1t1+(1-h1)h2t2+(1-h1)(1-h2)h3t3 (6)

=0.98t1+0.018t2+0.002t3

=8.04 µsec. – 3marks

Total memory cost -

Total cost=c1s1+c2s2+c3s3

=

=$15000 ---------- 3 marks

13 a) Explanation - 3 marks (3)

b) VLIW architecture + explanation - 4 marks (6)

VLIW pipelining with diagram - 2marks

PART C

Answer any two full questions,each carries 9 marks.

14 a) Transition diagram with all correct transitions– 3 marks (3)

b) Network design - 2 mark (6)

Routing + conflict - 3 marks

Blocking and Non blocking - 1 mark

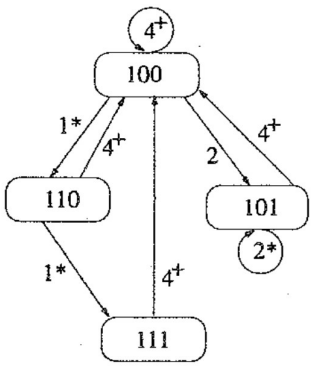
15 a) Synchronous Model with diagram - 1.5 marks (3)

Asynchronous Model with diagram - 1.5 marks

b) i) Forbidden latencies - 3 (6)

Collision vector - 100 - 1mark

ii) Transition diagram



- 2marks

iii) Simple cycles- 4, 2, (2,4), (1,4), (1,1,4)

Greedy cycles - 2, (1,1,4) - 1 mark

iv) optimal constant latency cycle -2

MAL- 2 - 1 mark

v) Throughput $=\frac{1}{2\times 20ns} = 25MOPS$ - 1mark

16 a) Explanation - 2 marks (4)

Directory structures - 2 marks

b) Dimension order routing - 2 marks (5)

Routing

r=$s \oplus d = 0010 \oplus 1001 = 1011$

routing- 0010->0011->0001->1001 - 2 marks

Intermediate nodes - 0011,0001 - 1 mark

PART D

Answer any two full questions, each carries 12 marks.

17 a) Tomasulo's Architecture - 3 marks (5)

Explanation - 2 marks

b) In order with example - 3.5 marks (7)

Out of order with example – 3.5 marks

18 a) Any three techniques - 9 marks (9)

b) Fine grain parallelism-explanation - 3 marks (3)

19 a) Static branch prediction - 3marks (6)

Dynamic branch prediction - 3marks

b) Architecture - 3 marks (6)

Explanation - 3 marks

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