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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION, MARCH 2016

Electronics & Communication Engineering

(VLSI & Embedded Systems)

04 EC6505— CMOS VLSI Design

Max. Marks : 60 Duration: 3 Hours

Part A

(Answer **ALL**, Each carrying 03 marks**)**

1. What is meant by noise margin? Define NM_L and NM_H using suitable diagram.
2. Explain cross-talk and what are the techniques used to control the cross talk in interconnect wires?
3. Draw the circuit diagram of a two-input depletion-load NOR gate and explain its working.
4. Obtain the circuit diagram and truth table of a CMOS SR latch based on NAND2 gates.
5. Realize AND and NAND gates using pass transistor logic.
6. Explain the concept of ratioed logic.
7. Explain the NORA CMOS logic circuit with an example.
8. Explain the monotonicity issue in dynamic CMOS logic.

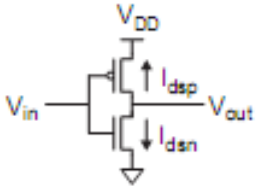
Part B

(Answer **ALL**, Each carrying 06 marks**)**

9. Draw the circuit diagram of a conventional BiCMOS inverter and explain the transient behavior during output pull-up and pull-down events.

OR

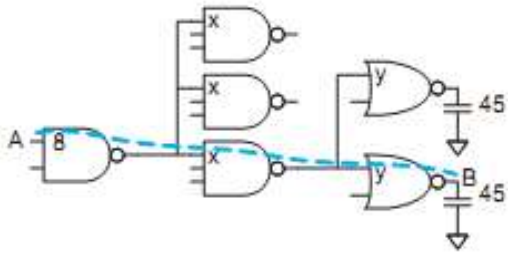
10. Graphically derive the DC transfer function (V_{out} vs. V_{in}) for the static CMOS inverter shown in figure below. Also explain the operation of the CMOS inverter in different regions.



11. Sketch a 2-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter. Compute the rising and falling propagation delays of the NOR gate driving h identical NOR gates using the Elmore delay model. Assume that every source or drain has fully contacted diffusion when making your estimate of capacitance.

OR

12. Estimate the minimum delay of the path from A to B and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8 λ of transistor width on the input and the output load is equivalent to 45 λ of transistor width.



13. Realize a one-bit full adder using the conventional CMOS design style.

Sum_out = A ⊕ B ⊕ C

Carry_out = AB + BC + AC

OR

14. Obtain the full-CMOS implementation of the following Boolean function:

$$Z = \overline{((A + B)(C + D)(E + F + GH))}$$

15. Explain the operation of NOR based implementation of the clocked JK latch circuit. Also draw the CMOS AOI realization of the JK latch.

OR

16. Draw the circuit diagram of a CMOS negative edge-triggered master-slave D flip-flop and explain the working.

17. Obtain the circuit diagrams of CPL NOR2, CPL NAND2 and CPL XOR gates. What are the design constraints for CPL design style?

OR

18. Draw and explain the circuit diagrams of two-input multiplexer and two-input XOR gate using transmission gate logic.

19. Explain the operation of a multiple-output domino CMOS gate with a suitable example.

OR

20. Implement the given function in dynamic CMOS logic and Domino CMOS logic.

$$Z = A\bar{B} + BC + \bar{C}$$