B

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION, FEB/MARCH 2016

Electronics & Communication Engineering

(VLSI & Embedded Systems)

04 EC6503—Advanced Digital Design

Max. Marks : 60 Duration: 3 Hours

PART A

Answer All Questions. All Questions Carry 3 marks Each.

1. Define Clock Skew.
2. Give an example for essential hazard.
3. Write down the behavioral description of a mod 13 synchronous counter.
4. Draw the Moore FSM controller state diagram for a serial adder.
5. Describe RTL design steps.
6. Convert the following c code in to high level state machine diagram

```
Inputs: uint A,B
Output: uint Carry
If (A=B) {
Carry =1;
}
else{
Carry = 0;
}
```

7. Draw Moore and Mealy state diagrams of 101 sequence detector.
8. Give an example for Operator Binding

PART B

Answer All Questions. All Questions Carry 6 marks each.

9. Write down the HDL code for a 4bit Adder/Subtractor.

or

10. Design a Mealy FSM to detect the occurrence of sequence 111 in a serial communication data line.
11. Design a basic memory cell with following conditions
    a. When SET =1 & RESET = 0 the Output is Q= 0;
    b. When SET = 0 & RESET = 1 the Output is Q= 1;
    c. When SET = 0 & RESET = 0 the Output is Undefined
    d. When SET = 1 & RESET = 1 the Output is Q = Q;

or

12. An unwanted glitch is present in a 3 input digital system which produces an output of logic '1' when following combination of input occurs.
    a. First and 3rd input is high with 2nd input is either zero *or* one.
    b. First input is zero and second is high with third is either zero *or* one.

    Analyse the reason for the glitch and realize a logic circuit by solving the issue.
13. Design a 4-bit register with clear, load, maintain present value, and shift right functions.

or

14. Design a display system to show the strength in a class room.
15. Design a controller for laser based distance measuring system

or

16. Distinguish between the Horizontal and Vertical micro codes of the given sequence of three micro operations of a Moore controller.
    0 -- > PC, PC + 1 -- > PC, ABUS -- > PC.

17. Design a Coffee Vending machine processing system using RTL design method with following specification. An input 'Start' becomes '1' for one clock cycle when coin is inserted, and two 8 bit inputs 'coin' and 'cost' indicates the value of the coin inserted and the cost of the coffee respectively. The processing system should set an output 'dispense' to logic '1' for one clock cycle if the coin value equal of exceeds the cost of the coffee.

or

18. Determine the maximum clock frequencies of 4 bit Ripple Carry Adder and Carry Look Ahead Adder. if it is realized by using the gates with 1ns delay. Assume all other delays are 0 .

19. Design an area optimized 3-tap FIR filter.

or

20. Design a pipelined adder to compute the sum of eight inputs on every clock cycles, where the sum is S= A + B + C + D + E + F + G + H + I. What is the latency and throughput of the adder if the single stage 8 bit adder has a delay of 4ns?