Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018
Course Code: EC204
Course Name: ANALOG INTEGRATED CIRCUITS (AE, EC)

Max. Marks: 100   Duration: 3 Hours

PART A
Answer any two full questions, each carries 15 marks.   Marks

1 a) Analyse the BJT differential amplifier pair under large signal operation and illustrate its transfer characteristics. (8)

   b) How to implement the instrumentation amplifier using three Op.Amp. Deduce the condition for ensuring high CMRR in the circuit? (7)

2 a) Using the small signal analysis, deduce the expression for CMRR and differential input resistance of the BJT differential amplifier from fundamentals. (9)

   b) What is the principle of operation of Wilson current mirror and its advantages? Deduce the expression for its current gain. (6)

3 a) Deduce the expression for the closed loop voltage gain, input resistance and output resistance for an op. amp. with voltage series feed back. (10)

   b) For an op-amp having a slew rate of 2V/μsec. What is the maximum closed loop voltage gain that can be used when the input signal varies by 0.5V in 10μsec? (5)

PART B
Answer any two full questions, each carries 15 marks.

4 a) How to realize Wein-Bridge oscillator using op. amp.? Derive the condition of oscillation and frequency of oscillation for the circuit. (8)

   b) Design a circuit to generate 1KHz triangular wave with 5V peak. (7)

5 a) Illustrate the working principle of the grounded load voltage to current converter and deduce the condition for its ideal current converter. (8)

   b) Design a fullwave rectifier to rectify an ac signal of 0.2V peak-to-peak. Explain its principle of operation. (7)

6 a) Derive the design equations for a second order Butterworth active low pass filter. (10)

   b) Design a Notch filter to eliminate power supply hum (50 Hz). (5)

P.T.O.

PART C
Answer any two full questions, each carries 20 marks.

7 a) Design a circuit to convert 1 KHz, 50% duty cyclesquare wave to 1 KHz, 30% duty cycle rectangular wave.   (7)

   b) How to configure fold back current limiting protection in 723 voltage regulator IC. Explain the circuit with internal block diagram of the IC.   (7)

   c) What is the principle of operation of successive approximation ADC?   (6)

8 a) Illustrate the principle of operation of PLL with its capture range and lock range   (7)

   b) How phase detector is implemented in digital PLL?   (5)

   c) Design a circuit to multiply the incoming frequency by a factor of 5 using 565 PLL.   (8)

9 a) Find out the Dynamic range, Full-scale value and Resolution of a 12 bit DAC having full-scale range 10V.   (5)

   b) Explain the working principle of R-2R ladder type DAC with circuit.   (6)

   c) What is the principle of operation of Dual slope ADC. Deduce the relationship between analogue input and digital output of the ADC.   (9)

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