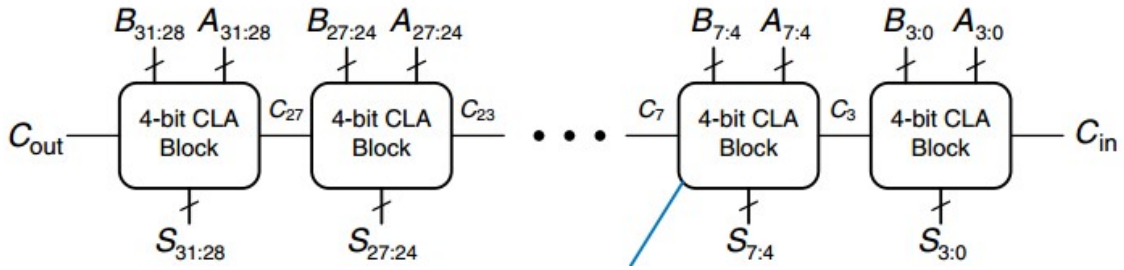
Computer Organization- Scheme for evaluaton

1. (a) Carry look Ahead Adder

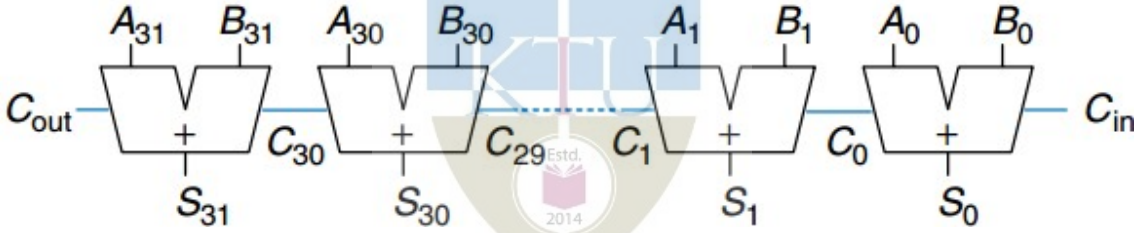


$$t_{CLA} = t_{pg} + t_{pg\_block} + \left(\frac{N}{k} - 1\right) t_{AND\_OR} + kt_{FA}$$

Delay Equation for Carry look ahead adder **(diagram 2 marks + Delay equation 2)**

Ripple carry Adder

$$t_{ripple} = Nt_{FA}$$



Ripple carry Adder **(diagram 2 marks + Delay equation 2)**

Description of working difference of both **(1 + 1)** **Total 10 marks**

(b) t pg = 200 ps ; t pg_block = 6x200 ps ; t AND_OR = 2 x 200 = 400 ps

t CLA = 200+ 1200 PS + (32/4 - 1) 400 + 4 X 400 (**2.5** marks)

$$t_{PA} = t_{pg} + \log_2 N(t_{pg\_prefix}) + t_{XOR}$$

t pg for Prefix adder

(**2.5** marks)

2. (a) Prefix Adder - Use equations mentioned below for construction

$$S_i = (A_i \oplus B_i) \oplus C_{i-1}$$

$$S_i = (A_i \oplus B_i) \oplus G_{i-1:-1}$$

$$G_{i:j} = G_{i:k} + P_{i:k} G_{k-1:j}$$

$$P_{i:j} = P_{i:k} P_{k-1:j}$$

(Writing correct equations **4** marks)

(drawing Prefix adder **4** marks + delay equation **2** marks) Total **10** marks

(b) Write R Type instruction definition (**2** mark) Register Type , Instruction format (**2** marks)

add $s0,$s1,$s2

op	rs	rt	rd	shamt	funct
0	$s1	$s2	$s0	0	32

(**1** mark) Total **5** marks

3. (a) 4- bit right shifter diagram (**5** marks)

(b) I - Type instructions , Use (**2** marks)

Instruction format (**3** marks)

(c) MIPS assembly code for

beq , bnr with example (**2.5 + 2.5** marks)

4. (a) MIPS addressing modes - 5 addressing modes (Each one with little explanation **8** marks. If only names are given only 3 marks)

(b) Pseudo instruction definition with an example (**2** marks)

MIPS instruction for mov $s1, $s2 (**3** marks) , working (**2** marks)

5.(a) Single cycle data path for subtracting two numbers

Step 1 .Fetching instruction from memory

step 2. Read source operand from the register file

step 3. Sign extend the immediate

step 4. Capture memory address

step 5. Write data back to the register file

step 7. Determine address of next instruction from PC

(Each step with explanation **1** mark, final complete diagram **3** marks) Total **10** marks

(b) Performance dependency - t c , critical path details(total 7 parameters at least 5 (5 x 1 = **5** marks)

6. (a) MIPS multi cycle processor with example. Example diagram (**6** marks)

Explanation (**4** marks)

(b) Each step 1 mark (5x 1= **5** marks)

7. (a) miss rate = 750/2000 = 0.375 = 37.5 % (**2.5** marks)

hit rate = 1-0.375 = 0.625=62.5 % (**2.5** marks)

(b) Virtual memory - explanation important points like virtual addresses, address translation, block size are to be checked and accordingly provide marks (**3** marks)

Address translation (**2** marks)

(c) Programmed I/O (2.5 marks), Interrupt driven I/O (**2.5** marks0

(d) SRAM, DRAM differences (**5** marks)

8.(a) Cache memory. what is it, why it is used. (**3** marks)

Different Cache mapping techniques (**7** marks)

(b) What is page table. Its uses (**2.5** marks)

Page table for address translation (**2.5** marks)

(c) DMA (**5** marks)

9. (a) Why standardization is needed in interfaces (**3.5** marks)

Details of PCI, SCSI, USB (each **1.5** marks) (Total **8** marks)

(b) Memory system hierarchy details (**3** marks)

Internal organization of a memory chip explanation (**4** marks)

(c) Different write policies in cache (**5** Marks)