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Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100   Duration: 3 Hours

PART A
Answer any two full questions, each carries 15 marks.   Marks

1 a) Convert the following   (8)

    (i) $(AB6)_{16}$ to Decimal   (iii) $(543.26)_{10}$ into Octal

    (ii) $(247.36)_8$ into Hexa Decimal   (iv) $(AF9.B0D)_{16}$ into Binary

  b) Consider the signed binary numbers A = 01000110 and B = 11010011 where B   (7)
     is in 2's complement form. Find the value of the following mathematical expression
    (i)   A + B

    (ii)   A - B

    (iii)   B - A

2 a) Hamming code was used to generate parity for a nibble. If received bit sequence   (8)
     is 0101010 then write correct bit sequence with (i) Even parity (ii) Odd parity

  b) Explain the operation of a 8x1 multiplexer and implement the following using   (7)
     an 8x1 multiplexer

     $F(A, B, C, D) = \sum m\ (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)$

3 a) Minimize the following logic function using K- maps and realize using NAND   (10)
     gates alone

     $F(A, B, C, D) = \sum m\ (0, 3, 5, 8, 9, 11,15) + d\ (2, 3)$

  b) Design a magnitude comparator to compare two 2-bit numbers $A = A_1A_0$ and   (5)
     $B = B_1B_0$

PART B
*Answer any two full questions, each carries 15 marks.*

4 a) Draw the circuit and explain the operation of TTL NAND gate   (10)

  b) Compare TTL, CMOS logic families in terms of fan-in, fan-out, supply voltage,   (5)
     propagation delay, power dissipation and noise margin

5 a) Implement the following function using PLA   (8)

        $F1(x, y, z) = \sum m\ (\ 1, 2, 4, 6\ )$

        $F2(x, y, z) = \sum m\ (0, 1\ , 6, 7)$

    b)   Explain a MOD 6 asynchronous counter using J K Flip Flop   (7)

6 a)   Design a 3-bit synchronous counter using D Flip Flop   (10)

    b)   Convert SR Flip Flop into J K Flip Flop   (5)

PART C
Answer any two full questions, each carries20 marks.

7 a)   Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control   (10)
         and explain its working.

    b)   Explain Moore and Mealy machine models. Compare the models   (10)

8 a)   Draw the logic diagram of 3 –bit Johnson counter and explain the working with   (10)

        truth table.

    b)   For the given state diagram, design a sequential circuit with D flip flops   (10)
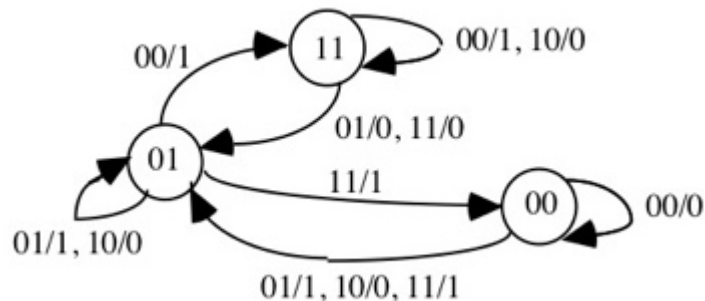
    (i) Construct the state table.

    (ii) Obtain the simplified input equations for all input flip flops and the simplified equation for the output.

9 a)   Minimize the state table using implication chart.   (10)

Present	Next state		Output (Z_1Z_2)	
state	X=0	X=1	X=0	X=1
0	0	1	00	00
1	4	2	00	00
2	7	1	00	00
3	2	6	01	10
4	6	5	10	00
5	3	4	01	11
6	1	6	01	10
7	3	8	10	00
8	8	7	01	11

    b)   Design a 101 sequence detector ,for overlapping case, using D Flip Flop   (10)

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