Reg. No._____ Name:_____

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

Course Code**: EE204**

Course Name**: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)**

Max. Marks: 100 Duration: 3 Hours

**PART A**

***Answer all questions; each question carries 5 marks***

1. Perform each of the following conversions:
   a) $(473)_{10}$ in to BCD code
   b) BAD in to ASCII
   c) $(289)_{10}$ in to hexadecimal
   d) $(110011.110)_2$ in to decimal
   e) $(53)_8$ in to hexadecimal
2. Simplify the following Boolean expression $\overline{AB} + \overline{AC} + \bar{A}\bar{B}\bar{C}$ .
3. Design a half adder circuit and realize using NAND gates only.
4. Realise a JK flip flop using SR flip flop.
5. Draw the logical diagram of a 4 bit ring counter using D flip flop.
6. What are the asynchronous inputs of a flip flop and discuss its functions.
7. Compare static RAM and dynamic RAM.
8. Write the VHDL code for the implementation of a full adder circuit.

**PART B**

***Answer any two questions; each question carries 10 marks***

9. Perform arithmetic operation using 2's complement method.
   a) -70 – 85 (5)
   b) 130 – 65 (5)
10. Using a 4 variable K map, simplify,

    $F(A,B,C,D) = \sum m(1,4,9,10,11,12,14) + d(0,8,13)$

    Realize the function using NAND gates only. (10)
11. a) Describe the operation of a basic parity generating and checking logical unit. (5)

    b) Compare the characteristics of TTL and CMOS logic families. (5)

## PART C

***Answer any two questions; each question carries 10 marks***

12. Design a MOD-12 asynchronous counter (ripple counter) using JK flip flop. Explain the working with truth table and timing diagram. (10)
13. a) Draw the block diagram of a 4 bit ALU, and explain it, showing its inputs and outputs. (5)
    b) Design a BCD to decimal decoder. (5)
14. What are fast adders? Design a 4 bit, carry look ahead adder, showing the logical diagram. (10)

## PART D

***Answer any two questions; each question carries 10 marks***

15. Design a counter to obtain the count sequence 2, 4, 3, 6, 2, 4, 3, 6… using JK flip flop. (10)
16. a) Compare the Moore and Mealy state machine models. (5)
    b) Compare PAL and PLA. (5)
17. With a neat block schematic, describe the working of a successive approximation ADC and illustrate it with a suitable example. (10)

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