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Reg. No.....

Name.....



B.TECH. DEGREE EXAMINATION, MAY 2014

Seventh Semester

Branch : Electronics and Communication Engineering / Applied Electronics and Instrumentation

VLSI TECHNOLOGY (LA)

(Old Scheme -- Prior to 2010 Admissions)

[Supplementary]

Time : Three Hours

Maximum : 100 Marks

Part A

Answer all questions.

Each question carries 4 marks.

1. Discuss the different steps in crystal shaping process.
2. Explain Fick's laws of diffusion.
3. Write a note on the fabrication of MOS resistors.
4. What are the differences in process steps in the fabrication of Si gate MOSFET compared to a metal gate MOSFET?
5. Briefly discuss constant field scaling.
6. Discuss the design rules for Vias and Metal 1.
7. Explain the transfer characteristics of an Inverter.
8. Explain the physical origin of latch up in CMOS transistors. How is it triggered and how can it be prevented?
9. Write a note on Channelling.
10. Discuss the need for device modelling. What are the minimum requirements to be taken care?

(10 × 4 = 40 marks)

Part B

Answer all questions.

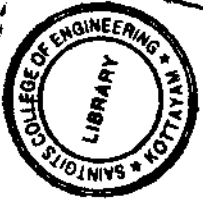
Each question carries 12 marks.

11. Explain the need for epitaxial growth. Discuss the CVD process for epitaxial growth.

Or

12. Explain the process of ion implantation in detail. What are its advantages?

Turn over



13. (a) Explain the different steps employed to control the V_T of a MOS structure.
(b) Write a note on IC cross over and Vias.

(9 + 3 = 12 marks)

Or

14. Explain the different isolation techniques used in IC fabrication. Give their features.
15. Explain a twin well CMOS process with neat sketches.

Or

16. Explain Short channel effects and Reverse short channel effects.
17. Draw the schematic and layout of a 2-input NOR gate.

Or

18. Explain the design of a 4-bit barrel shifter.
19. Explain the issues in a submicron process. What are the steps that can be taken to address these?

Or

20. Explain the doping process of a GaAs crystal.

[5 × 12 = 60 marks]