G 1084 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Sixth Semester

Branch : Electrical and Electronics Engineering

COMPUTER ORGANISATION (E)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. What is meant by hardwired control ?
2. What is micro programming and micro programmed control unit ?
3. What are the sequences of operations involved in processing an instruction constitutes an instruction cycle ?
4. Define micro programmed control.
5. Distinguish between asynchronies DRAM and synchronous RAM.
6. Explain cache memory.
7. Define hit rate and miss rate.
8. Explain memory interleaving.
9. What are the steps taken when an interrupt occurs ?
10. Define bus. What are the *three* types of buses ?

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Differentiate hardwire control and micro programmed control.

Or

12. Explain the organization of micro programmed control unit in detail.

Turn over

13. Discuss in detail serial and parallel adders.

Or

14. Explain multiplication and division operations using block schematic diagrams.

15. Explain different types of RAM memories.

Or

16. Explain : (a) ROM ; (b) PROM : (c) EPROM ; (d) E^2PROM.

17. Discuss the address translation mechanism and the different page replacement policies used in a virtual memory system.

Or

18. How a virtual address gets translated into physical addresses ? Explain in detail with neat diagram.

19. Explain the use of vectored interrupts in processors. Why is priority handling desired in interrupt controllers ? How do the different priority schemes work ?

Or

20. Design parallel priority interrupt for a system with eight interrupt source.

(5 × 12 = 60 marks)