Course	Course Name	L-T-P -	Yea	ar of			
code		Credits	Intro	luction			
EC206	COMPUTER ORGANISATION	3-0-0-3	20)16			
Prerequisite: EC207 Logic Circuit Design							
Course Objectives							
• To impart knowledge in computer architecture.							
• To	impart knowledge in machine language programming.						
То	develop understanding on I/O accessing techniques and me	emory strue	ctures.				
Syllabus							
Functional units of a computer, Arithmetic circuits, Processor architecture, Instructions and							
addressing modes, Execution of program, Micro architecture design process, Design of data path							
and control units, I/O accessing techniques, Memory concepts, Memory interface, Cache and							
Virtual memory concepts.							
Expected	d outcome .						
The stude	nts will be able to:						
i. Ur	i. Understand the functional units of a computer						
ii. Ide	lentify the different types of instructions						
iii. Ur	Jnderstand the various addressing modes						
iv. Ur	derstand the I/O addressing system						
v. Ca	tegorize the different types of memories						
Text Bo	ok:						
1. D	avid A. Patterson and John L. Hennessey, Computer Orga	anisation a	nd Desigr	n, Fourth			
Edition, Morgan Kaufmann							
2. D	avid Money Harris, Sarah L Ha <mark>rr</mark> is, Digital Design a	nd Comp	uter Arch	itecture,N			
K	aufmann – Elsevier, 2009						
References:							
1. Ca	rl Hamacher : "Computer Organization ", Fifth Edition, Mc	Graw Hil					
2. John P Hayes: "Computer Architecture and Organisation", Mc Graw Hill							
3. William Stallings: "Computer Organisation and Architecture", Pearson Education							
4. Andrew S Tanenbaum: "Structured Computer Organisation", Pearson Education							
5. Craig Zacker: "PC Hardware : The Complete Reference", TMH							
Course Plan							
Module	Contents		Hours	Exam			
			110015	Marks			
	Functional units of a computer						
	Arithmetic Circuits: Adder-carry propagate adder, Ripp	ole carry	4				
I	adder, Basics of carry look ahead and prefix adder, Su	ubtractor,	-				
	Comparator, ALU		15% 3				
	Shifters and rotators, Multiplication, Division						
	Number System: Review of Fixed point & Floating point	t number					
	system		1				
	Architecture : Assembly Language, Instructions, C	Operands,	2 15%				
т	Registers, Register set, Memory, Constants						
11	Machine Language: R-Type, I-Type, J-Type Inst	ructions,	3	1570			
	Interpreting machine language code		5				
FIRST INTERNAL EXAMINATION							
TTT	MIPS Addressing modes - Register only, Immediate, B	ase, PC-	3	1504			
	relative, Pseudo - direct		5	1,5 %			

	MIPS memory map, Steps for executing a program - Compilation,	, 2			
	Assembling, Linking, Loading Pseudoinstuctions, Exceptions, Signed and Unsigned instructions,				
	Floating point instructions	5			
IV	MIPS Microarchitectures – State elements of MIPS processor	1			
	Design process and performance analysis of Single cycle				
	processor, Single cycle data path, Single cycle control for R – type				
	arithmetic/logical instructions.		15%		
	Design process and performance analysis of multi cycle processor,				
	Multi cycle data path, Multi cycle control for R - type	3			
	arithmetic/logical instructions.				
SECOND INTERNAL EXAMINATION					
V	I/O system - Accessing I/O devices, Modes of data transfer,		20%		
	Programmed I/O, Interrupt driven I/O, Direct Memory Access,				
	Standard I/O interfaces - Serial port, Parallel port, PCI, SCSI, and				
	USB.				
	Memory system – Hierarchy, Characteristics and Performance analysis, Semiconductor memories (RAM, ROM, EPROM), Memory Cells – SRAM and DRAM, internal organization of a				
	memory chip, Organization of a memory unit.				
VI	Cache Memory – Concept/principle of cache memory, Cache size,		20%		
	mapping methods – direct, associated, set associated, Replacement	3			
	algorithms, Write policy- Write through, Write back.				
	Virtual Memory – Memory management, Segmentation, Paging,	3			
	Address translation, Page table, Translation look aside buffer.				
END SEMESTER EXAM					

Question Paper Pattern

The question paper shall consist of three parts. Part A covers I and II module, Part B covers III and IV module, Part C covers V and VI module. Each part has three questions, which may have maximum four subdivisions. Among the three questions, one will be a compulsory question covering both modules and the remaining from each module, of which one to be answered. Part A & Part B questions shall carry 15 marks each and Part C questions shall carry 20 marks each with maximum 80 % for theory and 20% for logical/numerical problems, derivation and proof.

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