Course	Course nome	L-T-P-	Ŋ	Year of		
code	Course name	Credits	Int	roduction		
AE308	ADVANCED MICROPROCESSORS	3-0-0-3		2016		
Prerequisite: AE305 Microprocessors & microcontrollers						
Course Objective						
• To familiarise the importance and applications of advance microprocessor						
To understand architecture of ARM processor						
To understand instruction set of ARM processor						
Syllabus	APLARDUL KA	A L A M	1			
Need of	advance microprocessors- RISC and CISC- ARM A	Architecture a	and Pr	ogrammers		
Model-	ARM Instruction set- C Programming for ARM-	Memory ma	anagen	nent units-		
Advanced Microprocessor Bus Architecture.						
Expected	outcome		<i>.</i> .			
	he students will have good idea about ARM processor	and its applic	cation.			
Text Books						
	1. Andrew N. Sloss, Dominic Symes, Chris Wright ARM System Developer's Guide,					
	Designing and Optimizing System Software, Elsevier					
2. N	indle edition	grumming Q	Агспи	ecture,		
3 St	eve Furber ARM System-on-chip Architecture 2nd F	dition Pears	on nul	dication		
4. W	illiam Hohl and Christopher Hinds, ARM Assembly L	anguage. Fun	ndamer	ntals and		
	<i>echniques.</i> 2nd edition. CRC Press.	unguage, i un	laamer	italis and		
Reference	e Books					
1. D	ouglas V.Hall, " <i>Microprocessors and Interfacing</i> ", Ta	ata McGraw I	Hill, II	Edition		
20	006					
2. M	ohamed Rafiquzzaman, "Microproce <mark>s</mark> sors and Micro	computer Bas	sed Sys	stem		
Design", II Edition, CRC Press, 2007						
Course Plan						
				Semester		
Module	Contents	Н	ours	Exam		
-	Fstd			Marks		
1	Introduction: Need of advance microprocessors, L	Difference 7		15%		
	between RISC and CISC, RISC Design philosoph	ny, ARM				
	Design Philosophy, History of ARM microprocess	or, ARM				
	processor family, Development of ARM architecture					
т	The APM Architecture and Programmers Model : T	be Acorp 7		150/		
11	PISC Machine APM Core data flow model Arc	hitectural		1370		
	inheritance The ARM7TDMI programmer's model	: General				
	numose registers CPSR SPSR ARM memory n	nan data				
	format load and store Architecture Core ex	tensions				
	Architecture revisions ARM development tool	ciensions,				
	i i i i i i i i i i i i i i i i i i i					
FIRST INTERNAL EXAMINATION						
III	ARM Instruction set: Data processing ins	tructions, 8		15%		
	Arithmetic and logical instructions, Rotate and barr	el shifter,				
	Branch instructions, Load and store instructions,	Software				
	interrupt instructions. Program status register ins	tructions.				

	Conditional execution, Multiple register load and store					
	instructions, Stack instructions, Thumb instruction set,					
	advantage of thumb instructions, Assembler rules and					
	directives, Assembly language programs for shifting of data,					
	factorial calculation, swapping register contents, moving					
	values between integer and floating point registers					
IV	C Programming for ARM: Overview of C compiler and	7	15%			
	optimization, Basic C data types, C Looping structures,	N.A.				
	Register allocations, function calls, pointer aliasing, structure	IV1				
	arrangement, bit fields, unaligned data and Endianness,	2				
	Division floating point. Inline functions and inline assembly.					
	Portability issues C programs for General purpose I/O					
	conorol nurnoso timor DWM Modulator LIADT					
	Interface SDI Interface ADC DAC					
	12C Interface, SFT Interface, ADC, DAC.					
	SECOND INTERNAL EXAMINATION		• • • •			
V	Memory management units: Moving from memory	7	20%			
	protection unit (MPU) to memory management unit (MMU),					
	Working of virtual memory, Multitasking, Memory					
	organization in virtual memory system, Page tables,					
	Translation look aside buffer, Caches and write Buffer, Fast					
	context switch extension.					
VI	Advanced Microprocessor Bus Architecture (AMBA) Bus	6	20%			
	System, User peripherals, Exception handling in ARM, ARM					
	optimization Techniques.					
FND SEMESTER EXAMINATION						

QUESTION PAPER PATTERN:

Maximum Marks:100

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2 together. Each question carries 15 marks and may have not more than four sub divisions.

Estd.

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

(15 x 2 = 30 marks)

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6 together. Each question carries 15 marks and may have not more than four sub divisions.

(20 x 2 = 40 marks)

Exam Duration: 3 Hours

2014