D **395B3** **Total pages: 2**

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SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SIXTH SEMESTER B.TECH DEGREE EXAMINATION(R,S), MAY 2024

Electronics and Communication Engineering

(2020 SCHEME)

Course Code : 20ECT312

Course Name : Digital System Design

Max. Marks : 100 **Duration:3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Sketch the ASM chart for a mod–3 down counter.
2. Explain the three state assignment rules with the help of an example.
3. Illustrate with example critical and non-critical races.
4. Explain dynamic hazards in combinational circuits with an example.
5. Differentiate fault and defect.
6. Describe the two types of stuck–at faults in digital circuits.
7. Implement a full subtractor using a PROM.
8. Implement the function f1 (x, y, z)=∑m (0, 1, 2, 6) using PLA .
9. Write the Verilog code for a JK flip flop.
10. Write the Verilog code for a 2-bit full subtractor.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. Design a CSSN using D-FF having a single input line ‘x’ in which binary symbols 1 and 0 are applied. The network is to produce an output ‘1’ coincident with the first 0 input symbol if it is preceded by exactly one or three 1 input symbols. All other times the output has to remain at 0. Write the proper sample sequence before starting the design. 14

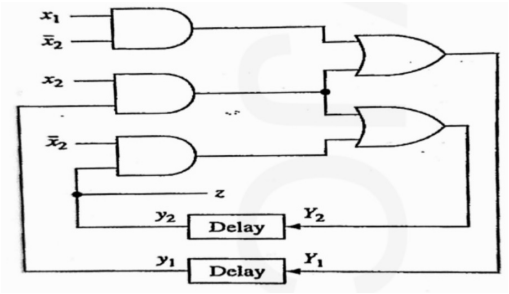
OR

12. Design a CSSN using T-FF having a single input line ‘x’ in which binary symbols 1 and 0 are applied. The network is to produce an output ‘1’ coincident with the first 0 input symbol if it is preceded by exactly one or three 1 input symbols. All other times the output has to remain at 0. Write the proper sample sequence before starting the design. 14

MODULE II

13. Design an ASC with two inputs x and y and with one output z. Whenever y is 1, the input x is transferred to z and when y=0, the output does not change for any change in x. 14

OR

14. 

14

Analyse the ASN by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in fundamental mode with the restriction that only one input variable can change value at a time.

MODULE III

15. Draw the logic diagram for the expression f = a.b'.c + (d'.e'). Find the test vectors for detecting the faults at input line a and d using Boolean difference method. 14

OR

16. Find the test vectors of all the sa0 and sa1 faults of the circuit whose Boolean function is f=x1x2+x1x3'x4'+x2x4 by Kohavi algorithm. 14

MODULE IV

17. Implement the following functions using PLA and obtain their compatibility matrix. f1(a,b,c,d) = ∑(1,2,3,4,5,6,8,10,13,15) f2(a,b,c,d) = ∑(2,9,10,12,14,15) 14

OR

18. In the context of PLA, explain the terms using appropriate examples: i) growth faults ii) shrinkage faults iii) appearance faults iv) disappearance faults. 14

MODULE V

19. Explain the architecture of XC 4000 FPGA family. 14

OR

20. Draw and explain the architecture of XC 4000 FPGA family. 14

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