B **514B1** **Total pages: 2**

Register No: …… Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R,S), MAY 2024

Computer Science and Engineering

(2020 SCHEME)

Course Code : 20CST202

Course Name : Computer Organization and Architecture

Max. Marks : 100 **Duration:3 Hours**

Scientific calculator and statistical table is allowed in the examination hall.

PART A

(Answer all questions. Each question carries 3 marks)

1. Enumerate the control signals needed for the execution of an unconditional branch.
2. Outline the steps involved in the execution of an instruction.
3. Write short note on accumulator register?
4. Differentiate between arithmetic and logic microoperations in the context of register transfer logic. Provide examples for each type of operation.
5. What is pipelining, and what are the benefits of implementing this concept in computer architecture?
6. Illustrate Read After Write (RAW) hazard with an example.
7. Explain PLA based control organization with the help of a diagram.
8. What is a microprogram sequencer, and how does it facilitate the execution of microinstructions in a microprogrammed control unit?
9. Explain the role of interrupt handlers in handling interrupts during I/O operations.
10. Differentiate between write-through and write -back protocol.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a)Draw the diagram of a multi-bus organization with 3 buses, write the control sequence for the instruction ADD R1,R2,R3 for the above mentioned multi-bus organization. 9

    b) What are condition codes? List the different condition codes. 5

OR

12. a)Identify the addressing modes that can be used for representing the following higher level language constructs in machine level. Illustrate each addressing mode using examples. 4
    i)Arrays
    ii)Pointers
    iii)Constants
    iv)Variables.

    b)Illustrate the single bus organization of processor unit with the help of suitable diagrams. How the following operations are handled in this organization by listing the control signals i)Transfer contents of register R1 to R2 10
    ii)ADD R6,R2.

MODULE II

13. a) Show and Explain the design of 4-bit status register. 6

b) Design a 4-bit combinational logic shifter which will perform the operation given below with two control variables H1&H0. 8

i) Shift left
ii) Shift right
iii) Clear
iv) Load all bits with 1

OR

14. Explain the basic concepts of ALU Design. Design and implement 4-bit ALU. 14

MODULE III

15. a)Multiply each of the following pairs of signed 2's-complement numbers using the Booth algorithm. In each case, assume that A is the multiplicand and B is the multiplier. i) A = 001011 and B = 011011 ii) A = 000111 and B = 000111 8

b) Design and explain the working of a 3*4 array multiplier. Find the number of AND gates and adders required for the same. 6

OR

16. a) Draw the flow chart of Booth's multiplication algorithm. Multiply (+24) and (-21) using Booth's multiplication algorithm. 8

b) Explain the principle of pipelining and discuss how it enhances the overall performance of a processor. Provide examples to support your explanation. 6

MODULE IV

17. With the help of a block diagram and function table, illustrate the functioning of a microprogram sequencer in a control unit designed for a processor. 14

OR

18. Discuss the advantages and disadvantages of using microprogram control in modern processor design by including considerations such as complexity, speed, and ease of modification. 14

MODULE V

19. Outline how Direct Memory Access is implemented? Differentiate between cycle stealing DMA and burst mode DMA. 14

OR

20. With the help of a diagram, explain the basic concepts of a memory system. 14

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