Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER INTEGRATED MCA DEGREE EXAMINATION (S), FEBRUARY 2024

(2020 SCHEME)

Course Code: **20IMCAT201**

Course Name: **Computer Organization**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. How do the functional units in a computer system work together?
2. Differentiate data bus, address bus and control bus.
3. Explain the fetch-decode-execute cycle in the execution of instructions.
4. What are the sequence of operations required to add the contents of register R1 to those of R2 and store the result in R3?
5. Explain the concept of sign and magnitude representation for signed numbers.
6. Perform the addition of two decimal numbers (-7) and (-4) using 2's complement method.
7. What is I/O-mapped I/O, and how does it differ from memory-mapped I/O?
8. Explain the purpose of the interrupt service routine (ISR)?
9. What is static memory? Explain.
10. Explain the two primary types of locality of reference.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Explain the concept of instruction pipelining and its advantages. (6)

OR

12. Compare and contrast immediate addressing and register addressing modes. Highlight the advantages and disadvantages of each. (6)

MODULE II

13. Explain how the CPU, memory, and I/O devices communicate through the system bus in a single bus architecture. (6)

OR

14. Compare and contrast hardwired control and microprogrammed control. (6)

MODULE III

15. What is carry lookahead adder, and how does it differ from traditional ripple carry adder? (6)

OR

16. How does Booth's algorithm handle signed binary numbers in multiplication? (6)

MODULE IV

17. Explain the need for DMA with a block diagram. (6)

OR

18. Explain the concept of instruction pipelining and its impact on the throughput of a processor. (6)

MODULE V

19. a) List the different types of ROM. (1.5)

b) What is the primary advantage of using SDRAM over asynchronous DRAM in terms of data transfer? (4.5)

OR

20. Differentiate associative and set associative cache mapping with examples. (6)

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