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SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIFTH SEMESTER B.TECH DEGREE EXAMINATION (R), DECEMBER 2023
ELECTRONICS AND COMMUNICATION ENGINEERING
(2020 SCHEME)

Course Code : 20ECT391

Course Name: FPGA Based System Design

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Describe FPGA design methodology.
2. Explain the procedural assignment statements in Verilog HDL.
3. Enlist the differences between PAL and PLA.
4. List the limitations of FPGA.
5. Describe the architecture of Look Up Table (LUT) with necessary diagrams.
6. Compare coarse-grained and fine-grained FPGA architectures.
7. Explain the importance of routing resources in FPGA.
8. Illustrate an application of FPGA in embedded system design.
9. List the four classes of commercially available FPGAs.
10. Sketch the general architecture of Actel FPGA.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Compare the different design options available in digital design. (9)
    b) Design a multiplexer using behavioral modelling in Verilog HDL. (5)

OR

12. a) Differentiate between mealy and moore models. (4)
    b) Define the term state machine. With an example describe the importance of state machines in digital system design. (10)

MODULE II

13. a) Implement the following truth table using PLA. Where A, B, C are the inputs and Y1, Y2 are the outputs. (10)

A	B	C	Y1	Y2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1

1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

b) Distinguish between FPGA and CPLD. (4)

OR

14. a) Draw and explain the structure of PAL. (4)
b) Implement the given Boolean function using PAL .
$X(A,B,C) = \sum_m(2,3,5,7)$
$Y(A,B,C) = \sum_m(0,1,5)$
$Z(A,B,C) = \sum_m(0,2,3,5)$ (10)

MODULE III

15. a) Sketch and explain the fundamental elements of FPGA architecture. (10)
b) Compare the logic cells of Actel and Xilix FPGA. (4)

OR

16. a) Sketch and explain the internal structure of CLB (configurable logic block). (10)
b) List the different programming technologies available in FPGAs. Explain anyone in detail. (4)

MODULE IV

17. a) What are the needs for partitioning. (4)
b) Explain different levels of partitioning. (10)

OR

18. a) Describe features of global routing and detailed routing. (10)
b) Illustrate an example of DSP system design using FPGA. (4)

MODULE V

19. a) Sketch and explain the general architecture of Xilinx FPGA. (10)
b) Compare the logic capacities of XC2000, XC3000, XC4000 (4)

OR

20. a) With a neat diagram explain the general architecture of Altera FPGA. (10)
b) Choose a sequential circuit and explain its design using FPGA. (4)

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