Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIRST SEMESTER M.TECH DEGREE EXAMINATION (Regular), DECEMBER 2023

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE102

Course Name: Advanced Digital Design

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. List the differences between mealy and moore machines.
2. Explain static hazards.
3. Design a 8 bit register with parallel load data input.
4. Explain micro programmed controller.
5. Describe high-level state machine.
6. Explain clock skew.
7. Describe visual method for two-level size optimization.
8. Define state encoding.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Design a circuit to detect 101 from given input data stream using mealy machine. (6)

OR

10. Minimize the function using Quin-McCluskey method F(A,B,C,D)= ∑(2,3,7,8,15). (6)

MODULE II

11. Explain races and cycles in digital circuits. (6)

OR

12. Explain Dynamic hazards in digital circuits. (6)

MODULE III

13. Design and sketch the circuit for a 4-bit parallel load shift right register. (6)

OR

14. Design a circuit using adders and logic gates to compute F=A*B where A and B are 4-bit numbers. (6)

MODULE IV

15. Explain RTL design process with an example. (6)

OR

16. Show the connection of controller and data path in a Soda dispensing system. Describe its significance in RTL design process. (6)

MODULE V

17. Explain clock jitter. (6)

OR

18. Describe any two methods for avoiding clock skew with neat sketches. (6)

MODULE VI

19. Draw the optimized logic circuit for the equation F(A,B,C,D)= ∑(0,2,6,7, 9,13) (a)using Quine-McCluskey method (b) using a K-map. Compare the above methods. (6)

OR

20. Explain two-level logic adder. (6)

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