Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED MCA DEGREE EXAMINATION (S), AUGUST 2023
(2020 SCHEME)

Course Code: **20IMCAT106**

Course Name: **Introduction to Digital Systems & Logic Designs**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert 1101101 and 11111 to decimal.
2. Convert decimal 125 and 479 to hexadecimal.
3. Prove (A + B) (A + C) = A + BC.
4. Implement NAND gate using NOR gate.
5. Write a short note on D flipflop.
6. Convert to standard SOP Y = A + BC.
7. Explain half subtractor with a diagram.
8. Design a 1-bit comparator.
9. Explain serial in parallel out shift register with a suitable diagram.
10. Compare synchronous and asynchronous counters.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Represent -17 in 8-bit sign magnitude, 1's complement and 2's complement form. (6)

OR

12. Do the following operations. (6)
    i. 1111 + 1111
    ii. 101 * 111
    iii. 1111 / 11.

MODULE II

13. State and prove Demorgan's Theorem. (6)

OR

14. Why is NAND gate called a universal gate? (6)

MODULE III

15. Minimize the boolean expression
f(A,B,C,D)= Σ{1,4,5,6,7,9,11,12,13,14,15}. (6)

OR

16. Illustrate the working of JK flip-flop with a neat diagram. (6)

MODULE IV

17. Design a full adder. (6)

OR

18. With a diagram, explain 4*1 multiplexer. (6)

MODULE V

19. Discuss the working of Serial In Serial Out shift register. (6)

OR

20. Explain the working of 3-bit asynchronous counter. (6)

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