G 815 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Eighth Semester

Branch : Electronics and Communication Engineering / Applied Electronics and Instrumentation / Electronics and Instrumentation Engineering

ADVANCED MICROPROCESSORS (L, A, S)

(Old Scheme—Supplementary/Mercy Chance—Prior to 2010 Admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. What are the functions of AO and $\overline{BHE}$ signals in 8086?
2. How does the DMA controller get the control of system buses?
3. What are the differences between MOV AX, 1234H and MOV AX, [1234H] instructions? Explain clearly.
4. If the SS and SP registers contain 4000H and 1234H respectively, what is the physical address of the top of the stack?
5. List the advantages of segment addressing of (i) real mode ; and (ii) protected mode.
6. Determine the physical address of the top of the stack in 80286 real mode, if SS = 4000H and SP = A900H.
7. Describe how the physical address is computed in 80386, if paging is enabled?
8. Distinguish between the real, protected and virtual real-modes of 80386.
9. Determine the physical addresses of the starting and ending memory locations of a segment in 80486 protected mode, if the segment descriptor holds the base address 00200000H and the limit 000FFH and if the 'G' bit is set.
10. List the flags in Pentium processor.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) Write instructions to enable and disable the INTR interrupts. Explain why the INTR interrupt is automatically disabled when an INTR interrupt is recognised. Indicate when and how the interrupt is re-enabled. (8 marks)

(b) Design an interfacing circuit for controlling NMI interrupts. (4 marks)

Or

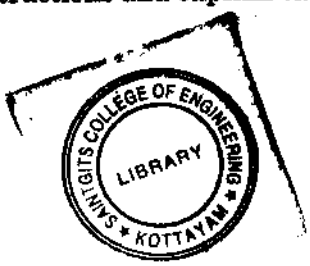
Turn over

12. (a) Design decoding logic for interfacing both input and output ports at I/O address 40H. (6 marks)

(b) Explain, in detail, the minimum mode 8086 bus timing for a memory read operation. (6 marks)

13. Determine the addressing modes of the following instructions and explain them :

(a) MOV CX, 4 [BX]
(b) SUB AX, AX
(c) INC AL
(d) STI
(e) IN AL, DX
(f) MOV AX, WORD PTR [BP] [DI]



(6 × 2 =12 marks)

Or

14. Write a 8086 ALP to compute simple interest for one year 10 principal amounts. The rate of interest is 10%. Write a subroutine for computing the interest. The subroutine should receive and send parameters through stack. (12 marks)

15. (a) What do you mean by a descriptor? Discuss the structure of a 80286 descriptor? (6 marks)

(b) Explain real and protected modes in 80286. (6 marks)

Or

16. (a) Explain Virtual Memory. How much virtual memory can an 80286 address? (6 marks)

(b) Differentiate between logical and physical addresses. (6 marks)

17. (a) Illustrate TSS in 80386 with neat block diagram. (6 marks)

(b) How 80386 can place into the protected mode operation for a more complex system using a TSS? (6 marks)

Or

18. (a) List and explain different data types supported by 80386 processor. (6 marks)

(b) Explain paging with reference to 80386. (6 marks)

19. (a) What is BIST? Explain 80486 burst. (5 marks)

(b) Explain the non-pipelined read cycle system timing for Pentium processor with neat circuit diagram and timing diagram. (7 marks)

Or

20. With neat block diagram, explain the PENTIUM CPU architecture and also explain the superscalar organisation. (12 marks)

[5 × 12 = 60 marks]