Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTER B.TECH DEGREE EXAMINATION (S), AUGUST 2023
ELECTRICAL AND ELECTRONICS ENGINEERING
(2020 SCHEME)

Course Code : 20EET206

Course Name: Digital Electronics

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert the given hexadecimal number to binary numbers (i) 901(ii) 1000 (iii)1111111.001.
2. Draw the internal diagram of a TTL NAND Gate.
3. Realize the function (AB +BC + AC) using NOR gates only.
4. What is the significance of K-map in Digital Electronics?
5. What is the role of parity generators in modern day communication?
6. Differentiate multiplexer and de-multiplexer.
7. What is the significance of race-around condition?
8. Realize a T flip-flop using a JK flip-flop.
9. Differentiate SAR ADC and flash ADC.
10. Justify reconfigurable feature of a FPGA.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Write notes on error detection codes, error correction codes and BCD. (9)
    b) 1's compliment method of subtraction is not preferred. Justify. (5)

OR

12. a) With proper examples, justify the statement "NAND gates and NOR gate are Universal gates". (9)
    b) Write short notes on IEEE floating point number system. (5)

MODULE II

13. a) Using K-Map, find the minimal POS expression if Y = ABC' + A'B'C + A'B'C' + ABC. (10)
    b) Write any four Boolean laws used in Digital Electronics. (4)

OR

14. a) With the help of K-map, simplify A'B'C + A'BC' + ABC + AB'C'. (10)
    b) Draw the diagram of a four-bit adder/subtractor. (4)

MODULE III

15. a) Realize a 8:1 multiplexer using 4:1 multiplexers. (7)
    b) Realize a 1:16 de-multiplexer using two 1:8 de-multiplexers. (7)

OR

16. Explain the significance of a BCD to Decimal decoder. With the help of truth table and K-map, design a BCD to Decimal decoder. (14)

MODULE IV

17. a) Design a Mod – 10 asynchronous Counter using JK Flip-flops. (9)
    b) What do you mean by a Mod N counter? Brief how the counter resets the count to zero after completion of one full cycle of N counts. (5)

OR

18. a) With neat diagram, explain the working of a Johnson's counter. (9)
    b) Differentiate SISO and SIPO registers. (5)

MODULE V

19. a) With suitable examples and diagrams, explain the working of R-2R ladder network DAC. (9)
    b) Differentiate Moore and Mealy machines. (5)

OR

20. a) Write short notes about (i) PAL (ii) PLA and (iii) FPGA. (9)
    b) Write a VHDL program for a full adder using Dataflow style of modeling. (5)

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