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Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Seventh Semester

Branch : Applied Electronics and Instrumentation Engineering

AI010 701—VLSI (AI)

(Improvement/Supplementary—2010 Admissions)

Time : Three Hours

Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. What is the need for epitaxial growth in IC fabrication?
2. What are the factors that prompts the use of HDL in digital design?
3. Write a note on Vias.
4. Write a note on poly Si depletion.
5. Discuss the features of strained Si.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Compare CVD with MBE.
7. Explain the VI characteristics of a CMOS inverter.
8. Write a note on junction isolation.
9. Write a note on MOS capacitors.
10. Write a note on Channeling effect.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Explain the different steps involved in a lithography process.

Or

12. Explain the Czochralski process. What are its features?

Turn over

13. Explain the need for scaling. Discuss the different approaches to scaling.

Or

14. Design a 2 input NAND gate using CMOS logic. Draw the stick diagram for the same. Realise a Biomos 2 input NAND gate and compare it with its CMOS counterpart.

15. Explain the different steps in the fabrication of a BJT.

Or

16. Explain the fabrication of monilithic resistors and capacitors.

17. Explain the twin well process for fabrication of a CMOS transistor.

Or

18. (a) Explain latchup in CMOS technology. (5 marks)

    (b) Compare a metal gate CMOS to a Si gate CMOS. (7 marks)

19. Explain the crystal structure and doping process in GaAs technology.

Or

20. Explain strained Si technology. How can such a crystal be achieved? How can it be used to build devices?

[5 × 12 = 60 marks]