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SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), MAY 2023

COMPUTER SCIENCE AND SYSTEMS ENGINEERING

(2021 Scheme)

Course Code: **21SE201**

Course Name: **Computer System Design and Architecture**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. State Amdahl's law.
2. An instruction pipeline consists of 4 stages:

   Fetch(F), Decode operand field (D), Execute (E), and Result-Write (W). The five instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below.

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

   Find the number of clock cycles needed to perform the 5 instructions.
3. With a neat sketch explain memory hierarchy design.
4. Assume that for a certain processor, a read request takes 50ns on a cache miss and 5 ns on a cache hit. Suppose while running a program, it was observed that 80% of processor's read requests result in cache miss. Find the average access time in nanoseconds.
5. Define mirroring. What are its advantages and disadvantages?
6. Narrate the features that RAID provides to a user.
7. Justify the statement "*The designer prefer a distributed shared memory architecture to that of a centralized storage facility*"
8. Define Software Multithreading.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Illustrate Von Neumann Architecture. (6)

OR

10. Explain the different Flynn's taxonomies of computer architecture. (6)

MODULE II

11. Discuss in detail on various hazards in Pipelining. (6)

OR

12. Illustrate Tomasulo algorithm for the following code
(Assume: ADD instruction will take TWO clock cycle and MUL instruction will take THREE clock cycle)
w: ADD R4,R0,R8
x: MUL R2,R0,R4
y: ADD R4,R4,R8
z: MUL R8,R4,R2 (6)

MODULE III

13. A user need to design a system which is capable of processing multiple data over a single instruction that been given to the system. Suggest a suitable processor that meets the requirement and illustrate it's working. (6)

OR

14. With a neat sketch explain the working of GPU. What are its advantages to that of a normal processing unit? (6)

MODULE IV

15. A cache designer like to increase the performance of a cache by reducing the miss rate, as an expert in this area suggest the designer some ideas to achieve the goal. (6)

OR

16. Define the following terms in cache organisation mechanisms
a) Direct mapping
b) Set associative mapping
c) Fully associative mapping (6)

MODULE V

17. Explain the different types of storage devices in a system. (6)

OR

18. Draw a neat sketch for the following RAID
a) RAID 0+1 b) RAID 1+0 (6)

MODULE VI

19. Illustrate the working of multi core architecture with a neat diagram. (6)

OR

20. With neat sketch explain Distributed Shared Memory and Centralized Shared Memory system with advantages and disadvantages. (6)

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