Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED MCA DEGREE EXAMINATION (R), MAY 2023

(2020 SCHEME)

Course Code: **20IMCAT106**

Course Name: **Introduction to Digital Systems & Logic Designs**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert $(1111111)_2$ and$(1011)_2$ to decimal.
2. Convert $(123ABCD)_{16}$ to decimal.
3. Design XNOR using basic logic gates.
4. Prove A+A'B=A+B.
5. Write a short note on JK flipflop.
6. Compare latches and flipflops.
7. Draw the logic circuit of half adder.
8. Write a short note on combinational circuits.
9. Explain SoC model.
10. What are the different types of shift registers?

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Represent -25 in 8-bit sign magnitude, 1's complement and 2's complement form. (6)

OR

12. a) Write a short note on octal numbers. (2)

    b) Convert **$(321)_8$** to decimal form. (4)

MODULE II

13. Construct NAND and NOR along with truth table. (6)

OR

14. State and prove Demorgan's theorem. (6)

MODULE III

15. Minimize the following boolean function using K-map. (6)
F(A, B, C, D) = Σm(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)

OR

16. Illustrate the working of SR flipflop with a neat diagram. (6)

MODULE IV

17. Design a full subtractor. (6)

OR

18. Explain decimal to BCD encoder with the logic symbol. (6)

MODULE V

19. Write note on Serial-In Parallel-Out shift Register. (6)

OR

20. Compare synchronous and asynchronous counters. (6)

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