Register No.: ·····

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

Name:

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (S), FEBRUARY 2023 ELECTRONICS AND COMMUNICATION ENGINEERING

(2020 SCHEME)

Course Code : 20ECT201

Course Name: Solid State Devices

Max. Marks : 100

PART A

(Answer all questions. Each question carries 3 marks)

- 1. Distinguish between elemental and compound semiconductors with example.
- 2. Sketch the energy band diagram of the given semiconductors in equilibrium.i) Intrinsic, ii) n-type and iii) p-type
- 3. List the assumptions taken for the derivation of diode current equation.
- 4. Describe the significance of quasi fermi level.
- 5. Explain emitter injection efficiency and base transportation factor in a BJT.
- 6. Explain the Early effect mechanism in BJT.
- 7. Write the expression for drain current at linear region and saturation region for a MOSFET.
- 8. Define threshold voltage of a MOS capacitor.
- 9. Discuss channel length modulation in MOSFET.
- 10. Explain the principle of operation of FinFET.

PART B

(Answer one full question from each module, each question carries 14 marks) MODULE I

- 11. a) Derive the equation for hole concentration in a semiconductor under (8) thermal equilibrium.
 - b) Calculate the thermal equilibrium electron and hole concentration for a Si semiconductor with band gap 1.12 eV, Fermi level 0.25 eV (6) below conduction band, Nc= $2.8 \times 10^{19} \text{ cm}^{-3}$ and Nv= $1.04 \times 10^{19} \text{ cm}^{-3}$.

OR

- 12. a) A silicon sample doped with $2x10^{16}$ cm⁻³ of Boron atoms. Determine,
 - i) The equilibrium electron and hole concentrations
 - ii) Position of fermi energy level in the band diagram.
 - Given $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ for Silicon at 300K.
 - b) Explain Fermi Dirac distribution function and position of Fermi level in intrinsic and extrinsic semiconductors with diagram. (7)

Duration: 3 Hours

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(7)

MODULE II

- 13. a) Explain the variation of mobility with temperature and doping. (6)
 - b) Derive the continuity equation under steady state conditions, assuming the semiconductor is long and no drift current is present. (8)

OR

- 14. a) Derive the steady state diffusion equation in semiconductors. (7)
 - b) A potential of 100mV is applied across a semiconductor bar, and the resulting current is 1mA. A magnetic field of 10⁻⁴Wb/cm² is applied perpendicular to the semiconductor bar. The hall voltage measured is -2mV. The dimensions of the bar are width = 0.01mm, length = (7) 5mm and thickness = 10 x 10⁻⁶m. find i) the type of the semiconductor bar. ii) the concentration and the mobility of majority carriers.

MODULE III

- 15. a) Explain the behavior of a metal and an n-type semiconductor (7) junction with the help of energy band diagrams.
 - b) Derive the expression for ideal diode equation.

OR

- 16. a) Derive the equation for the contact potential of a PN junction under (8) thermal equilibrium.
 - b) Determine the base transport factor and the emitter injection efficiency of a p-n-p transistor with parameters, $I_{Ep} = 2mA$, $I_{En} = (6) 0.01mA$, $I_{Cp}=1.98mA$ and $I_{Cn}=0.001mA$.

MODULE IV

- a) Sketch the energy band diagrams of an ideal MOS capacitor under i) equilibrium ii) depletion iii) inversion and iv) strong inversion (7) conditions.
 - b) Derive the expression for drain current of a MOSFET in the two regions of operation. (7)

OR

- 18. a) A silicon n channel MOSFET has $\mu n = 600 \text{cm}^2/\text{V}$ s, $C_{\text{ox}} = 1.2 \text{ x } 10^{-7}$ F/cm², W = 50 μ m, L=10 μ m and V_{TH} = 0.8V. Calculate the drain (7) current when i) V_{GS}=2V and V_{DS}=1V ii) V_{GS} = 3V and V_{DS}= 5V.
 - b) Explain the operation of an n-channel MOSFET with necessary diagrams also describe its characteristics. (7)

MODULE V

19. a) Explain the concepts of velocity saturation and hot carrier effects in (7)

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a MOSFET b) Explain DIBL and its effects in MOSFET (7) **OR** 20. a) Explain the challenges in device scaling? (6) b) Describe the structure and working of a FINFET with suitable (8) diagrams.

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