G 406 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Sixth Semester

Applied Electronics and Instrumentation

AI 010 606 L 03—DIGITAL SYSTEM DESIGN (Elective -I) (AI)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Failed]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. State the difference between PROM and EPROM.
2. Distinguish between Moore and Mealy machine.
3. Describe the main features of IIC bus.
4. Explain the use of PROCESS in VHDL.
5. List the various operators used in VHDL.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Implement the following functions using ROM

   $F_1(A, B, C) = \sum m(0, 1, 3, 7)$ and $F_2(A, B, C) = \sum m(0, 2, 6)$.

7. Explain RS 232 standard.
8. Draw the state diagram of a sequence detector to detect the sequence 11010.
9. Differentiate between structural and behavioural modelling.
10. Explain the usage of attributes in VHDL.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Differentiate between PLA and PAL Implement the following functions using a suitable PLA.

$F_1(A, B, C, D) = \sum m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$.

$F_2(A, B, C, D) = \sum m(2, 3, 5, 6, 7, 10, 11, 14, 15)$.

$F_3(A, B, C, D) = \sum m(6, 7, 8, 9, 13, 14, 15)$.

(12 marks)

Or

12. Explain how FPGA can be used to implement logical functions with the help of its architecture. (12 marks)

13. Explain the features of PCI, its applications and advantages in detail. (12 marks)

Or

14. **Explain** any *one* **Bus Interface IC in detail.** (12 marks)

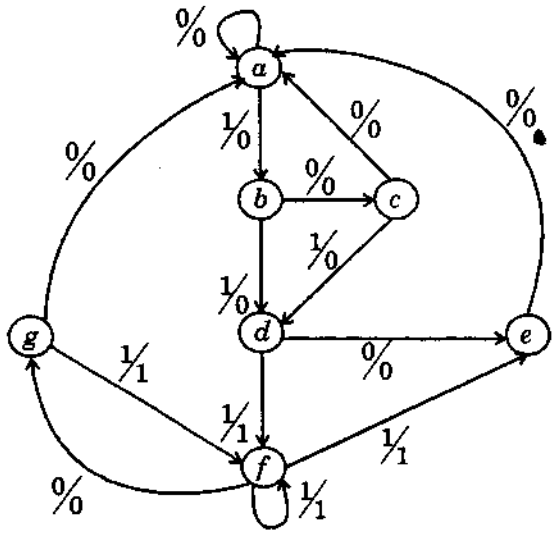
15. (a) Describe the design procedure of a finite state machine. (6 marks)

(b) Draw the SM chart for a Binary Multiplies. (6 marks)

Or

16. (a) Explain the process to find two equivalent states. (5 marks)

(b) Reduce the State diagram.



(7 marks)

17. (a) Write a VHDL description for n-bit binary adder using structural modelling. (6 marks)

(b) Implement a 1 : 4 demultiplexes using behavioural modelling. (6 marks)

Or

18. Draw the design flow diagram in VLSI and explain. (12 marks)

19. (a) Write the behavioural description of JKFF with active low preset and clear $1/ns$. (6 marks)

(b) Write a VHDL program for implementation of a 4-bit counter. (6 marks)

Or

20. (a) Differentiate between RAM and ROM. (6 marks)

(b) Write a VHDL code for ROM realization for the data storage of ten 4-bit numbers. (6 marks)

[5 × 12 = 60 marks]