Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (Regular), DECEMBER 2022
ELECTRICAL AND ELECTRONICS ENGINEERING
(2020 SCHEME)

Course Code : 20EET205

Course Name: Analog Electronics

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Explain why a fixed bias circuit is not widely used in amplifiers, despite its simplicity.
2. Define thermal runaway.
3. Compare JFET with MOSFET.
4. Explain pinch off voltage of JFET using drain characteristics.
5. Draw the circuit of two stage RC coupled amplifier and briefly explain loading effect.
6. State and explain Barkhausen's criterion of oscillation.
7. Outline the virtual ground concept in Op-Amp.
8. Explain the concept of CMRR and Slew rate of 741 Op-Amp.
9. Draw the circuit diagram of an ideal integrator and derive the expression for output voltage.
10. Explain voltage level detector circuit with neat diagram. Draw the output waveform considering that the input is $V_{in}=10\sin\omega t$ and $V_{ref}=4V$.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Determine the voltage gain, current gain, input impedance and output impedance of the common emitter amplifier circuit driving a load of 5kΩ. It is supplied by a signal source of internal resistance 10kΩ. The hybrid parameters of the transistors are h_{ie}=1100Ω, h_{re}=2.5×10−4, h_{fe}=50, h_{oe}=25 μʊ. (8)

    b) Analyze the working of collector to base bias configuration of BJT and derive the expression for stability factor. (6)

OR

12. a) Determine the following parameter for the fixed bias configuration of transistor amplifier. i) I_C, ii) V_{CC}, iii) R_B, iv) β (6)
    Given Rc = 2.5kΩ, IB = 20μA, I_E = 3mA, V_{CE} = 6.5V

b) List the factor affecting the stability of operating point of a transistor. Derive the expression for stability of voltage divider bias. (8)

MODULE II

13. a) Sketch the constructional features of a JFET. (4)
b) Draw and explain the working of common drain FET amplifier with voltage divider bias arrangement using small signal AC equivalent circuit. Also derive the expression for voltage gain, input impedance and output impedance. (10)

OR

14. a) Explain the construction and working of Depletion type MOSFET. (6)
b) With suitable circuit diagrams, explain the effect of internal capacitance during high frequency operation of CE amplifier. (8)

MODULE III

15. a) Describe the operation of class B push pull power amplifier and determine its maximum power conversion efficiency. (8)
b) Compare positive and negative feedback in amplifiers. (6)

OR

16. a) With a neat circuit diagram, explain RC phase shift oscillator using BJT. Derive an expression for frequency of oscillation. (8)
b) Examine the advantages and disadvantages of transformer coupled multi stage amplifier. (6)

MODULE IV

17. a) Draw the circuit of an inverting amplifier and obtain the expression for its closed loop gain. Also design an inverting amplifier with gain 12. (8)
b) Summarize the characteristics of ideal and practical Op-Amps. (6)

OR

18. a) Explain the working of non-inverting summing amplifier using Op-Amp? Also derive the expression for output voltage. (8)
b) Design an op-amp circuit to obtain an output of $Vo=-[3V_1+2V_2+0.5V_3+5V_4]$, where V_1, V_2, V_3 and V_4 are the inputs to op-amp. (6)

MODULE V

19. a) Explain the working of an ideal differentiator using op-amp and derive the expression for output voltage. Draw the output waveform of the differentiator when input is square wave. (9)
b) List disadvantages of an ideal integrator and give the details of modifications done in practical integrator to overcome this? (5)

OR

20. a) Illustrate the working of an Astable multivibrator using 555 IC. Also derive the expression for frequency of oscillation. (8)

b) Design an astable multivibrator using 555 timer IC to generate an output signal with frequency 2kHz and 60% duty cycle. (6)

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