Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTER B.TECH DEGREE EXAMINATION (S), SEPT 2022

COMPUTER SCIENCE AND ENGINEERING

(2020 SCHEME)

Course Code : **20CST202**

Course Name: **Computer Organization and Architecture**

Max. Marks : **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Differentiate between Big-endian and Little-endian byte addressing formats.
2. Write the three-address, two-address and one-address representations of the operation below with relevant assumptions:

   $C \leftarrow [A] + [B]$
3. Write a short note on status register.
4. Write down different operations that are considered for the design of accumulator circuit.
5. List out various pipeline conflicts.
6. Distinguish between Data Hazards and Instruction hazards.
7. Illustrate divide overflow with an example
8. What are micro-instructions? Explain with example.
9. Explain any two interrupt priority schemes
10. Describe about flash memory.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Illustrate the advantages of using multiple bus organization over single bus organization with the help of a sample instruction execution. (10)

    b) Give the sequence of control steps required to perform the operation: Add [R3], R1 in a single-bus organization. (4)

OR

12. a) What are addressing modes? List out various addressing modes and explain with an example for each. (10)

    b) Give the relevance of MAR, PC and IR in a typical computer system with neat diagram. (4)

MODULE II

13. a) Discuss the major operations that can be performed by a parallel adder in the design of arithmetic circuit. (9)

    b) Explain scratchpad memory with the help of a neat diagram. (5)

OR

14. a) Draw a labelled block diagram of a processor unit with seven registers R1 to R7, a status register, shifter with 3 selection variables, ALU with 3-selection variables and C_{in}. Also explain about the functions of selection variables. (9)
    b) Explain about design of a combinational logic shifter. (5)

MODULE III

15. a) Write down the algorithm and draw the flowchart for Booth multiplication. (8)
    b) Multiply the following pair of signed 2's complement number using Booth's algorithm. Assume A is the multiplicand and B is the multiplier. (6)
    A=010111 B=110110

OR

16. a) Differentiate between arithmetic pipelining and instruction pipelining with necessary diagrams. (8)
    b) Explain about restoring division algorithm with one example. (6)

MODULE IV

17. a) Briefly explain about the components of micro programmed control unit with a neat sketch (10)
    b) Distinguish between vertical and horizontal organization of control signals. (4)

OR

18. a) With the help of a diagram establish the functioning of microprogram sequencer in a microprogram-controlled processor. (10)
    b) Explain how control signals are generated in one flip flop per state control logic with the help of a diagram. (4)

MODULE V

19. a) Explain the different ways in which interrupt priority schemes can be implemented. (10)
    b) Compare and contrast between SRAM and DRAM. (4)

OR

20. a) Explain about cache memory mapping functions. (10)
    b) Compare the two main modes of DMA transfer. (4)

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