Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED M.C.A DEGREE EXAMINATION (S), SEPT 2022

(2020 SCHEME)

Course Code: **20IMCAT106**

Course Name: **Introduction to Digital Systems & Logic Designs**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Explain 1's complement and 2's complement of a binary number with an example.
2. Convert $(435)_8$ to hexadecimal.
3. State De Morgan's theorem.
4. Which gates are called universal gates? What are its advantages?
5. Compare latches and flip-flops.
6. Explain SOP and POS form.
7. Compare half adder and half subtractor.
8. Find the number of 2 X 1 multiplexers required to implement a 16 X 1 multiplexer.
9. What are the differences between synchronous and asynchronous counters?
10. Explain Parallel-In Parallel-Out registers.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Compute the following.
    a) $(111)_2 * (101)_2$
    b) $(111101)_2 \div (100)_2$ (6)

OR

12. Represent the following binary numbers in 8-bit sign magnitude form, 1's and 2's compliment form.
    a) 01101
    b) 010111
    c) 10111
    d) 1101010 (6)

MODULE II

13. State and prove basic laws of boolean algebra. (6)

OR

14. a) Simplify F = x'yz + x'yz' + xz
b) Prove that x'y'z' + x'yz' + xyz' = x'z' + yz' (6)

MODULE III

15. Express the boolean function F = A + B' C as a sum of minterms. (6)

OR

16. Express the boolean function F = X Y + X' Z as a product of maxterms. (6)

MODULE IV

17. Explain full adder with the help of a truth table. Design its circuit diagram using basic logic gates. (6)

OR

18. Explain the working of a 4*1 multiplexer with a neat diagram. (6)

MODULE V

19. With a neat diagram, explain the working of Parallel In Serial Out shift register. (6)

OR

20. Design a binary 4-bit asynchronous up counter using D flip flops. (6)

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