Register No.: …… Name: ……

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), JULY 2022

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: **21VE204-E**

Course Name: **Physical Design and Verification**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Summarize the frontend flow in IC design.
2. Demonstrate setup and hold violations.
3. Enumerate the various constraints of routing.
4. Explain the various types of power cell management associated with power planning.
5. Define clock cross talk with an example.
6. Illustrate clock tree synthesis flow.
7. Explain cross clock balancing.
8. Describe logical equivalence checking associated with physical verification.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

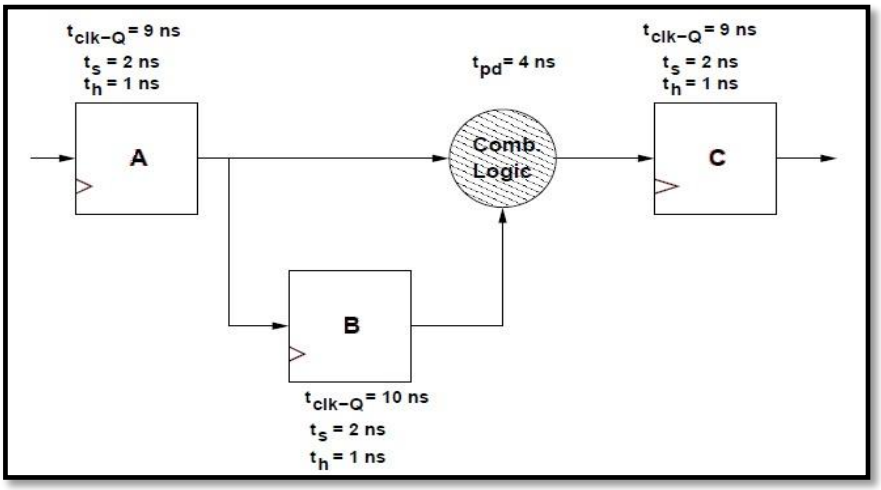
9. Demonstrate the flow of synthesis with an example. (6)

OR

10. Summarize backend flow in IC design. (6)

MODULE II

11. Analyze the following circuit and calculate the maximum clock frequency that can be given.



(6)

OR

12. Illustrate static timing analysis with relevant diagrams. (6)

MODULE III

13. Demonstrate routing steps with relevant sketches. (6)

OR

14. Illustrate the following (a) Detail routing (b) Post route optimization (6)

MODULE IV

15. Explain congestion. Mention the methods for controlling congestion during placement. (6)

OR

16. Describe floor planning in physical design with relevant diagrams. (6)

MODULE V

17. Illustrate clock tree optimization technique with an example. (6)

OR

18. With necessary diagram explain clock tree exceptions. (6)

MODULE VI

19. Enumerate the significance of TCL scripting in physical design with any two examples. (6)

OR

20. Explain synchronous clock balancing with necessary waveforms. (6)

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