Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH. DEGREE EXAMINATION (Regular), JULY 2022

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: **21VE202**

Course Name: **Advanced CMOS VLSI Design**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Describe the limits of low power and low voltage operation.
2. An NMOS transistor has$V_{to} = 0.8V$, $2\phi_f = 0.7V, and\ \gamma = 0.4\ V^{\frac{1}{2}}$. Find V_t when V_{SB} = 3 V.
3. Describe stacking effects to reduce leakage current in CMOS circuits.
4. Define "Charge-Sharing Problem" in a CMOS dynamic logic circuit. How it can be overcome.
5. Apply CPL technique to implement XOR/XNOR gate.
6. Sketch the circuit diagram of a 3-input NAND gate in NMOS logic and pseudo-NMOS logic.
7. Enumerate the advantages of 6T SRAM cell compared to 4T SRAM.
8. Identify the major sources of power wastage in SRAM.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Describe with the aid of diagrams and equations, how velocity saturation affect the performance of a submicron channel device. (6)

OR

10. Explain impact ionization in short channel MOSFET with diagram. (6)

MODULE II

11. List the different components of power dissipation in CMOS circuit. Show that switching power dissipation is directly proportional to the square of supply voltage. (6)

OR

12. Write the expression for subthreshold leakage current. Explain the relation between subthreshold leakage and subthreshold swing. (6)

MODULE III

13. Explain the supply voltage scaling techniques to reduce power reduction. (6)

OR

14. Differentiate VTCMOS and MTCMOS for leakage power reduction. (6)

MODULE IV

15. List the disadvantages of domino logic. Implement Y = AB+ CD + EF using the domino logic. (6)

OR

16. Illustrate the topology of a Precharged - high Differential Current Switch Logic. (6)

MODULE V

17. Sketch and explain the working of a 2 input XOR gate using DCVS logic. (6)

OR

18. List the advantages and limitations of pass transistor logic circuits. How the limitations can be overcome. (6)

MODULE VI

19. Explain the various low-voltage low-power SRAM cell design with neat diagram. (6)

OR

20. Explain with circuit diagram how the read, write and hold operations are performed in SRAM. In what way the DRAMs differ from SRAMs. (6)

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