Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED M.C.A DEGREE EXAMINATION (R), JULY 2022
(2020 SCHEME)

Course Code: **20IMCAT106**

Course Name: **Introduction to Digital Systems & Logic Designs**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert $(110010)_2$ and $(11111)_2$ to Decimal.
2. Convert the hexadecimal number $(ACE)_{16}$ to decimal number.
3. Explain the laws of Boolean algebra.
4. Prove that A'B+AB'+AB=A+B.
5. Explain SR flip flop.
6. Convert AB+AC to standard SOP.
7. Draw the circuit diagram of full adder.
8. Explain multiplexer with an example.
9. Write short note on Serial In Serial Out shift register.
10. What is asynchronous counter?

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

11. Represent -56 in 8-bit sign magnitude, 1's complement and 2's complement form. (6)

OR

12. Explain arithmetic operations on binary number system with example. (6)

MODULE II

13. State and prove Demorgan's theorem. (6)

OR

14. Explain universal gates. (6)

MODULE III

15. Using Karnaugh map, convert the following standard POS expression into a minimum POS expression, a standard SOP expression and a minimum SOP expression. (6)

(A'+B'+C+D)(A+B'+C+D)(A+B+C+D')(A+B+C'+D')(A'+B+C+D')(A+B+C'+D)

OR

16. Illustrate the working of J-K flip flop with a neat diagram. (6)

MODULE IV

17. Design a full subtractor. (6)

OR

18. With a diagram, explain 4 X 1 demultiplexer. (6)

MODULE V

19. Explain Parallel In Serial Out and Parallel In Parallel Out registers. (6)

OR

20. Compare synchronous and asynchronous counters. (6)

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