# SAINTGITS COLLEGE OF ENGINEERING KOTTAYAM, KERALA <br> (AN AUTONOMOUS COLLEGE AFFILIATED TO 

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# FIRST SEMESTER M.TECH. DEGREE EXAMINATION, MARCH 2021 VLSI AND EMBEDDED SYSTEMS 

Course Code: 20ECVET103<br>Course Name: ADVANCED DIGITAL DESIGN

Max. Marks: 60

## Duration: 3 Hours

## PART A

## (Answer all questions. Each question carries 3 marks)

1. Define Clock Skew and briefly explain the different types with illustrations.
2. Differentiate between critical and non critical races with examples.
3. Design a 4 bit by 4 bit array style multiplier with a neat diagram.
4. Describe the different steps in controller design.
5. Assuming an inverter has a delay of 1 ns , all other gates have a delay of 2 ns , and wires have a delay of 1 ns , determine the critical path for a 8 bit ripple carry adder.
6. Differentiate between high level state machine and finite state machine.
7. Perform two- level logic size optimization for $\mathrm{F}(\mathrm{a}, \mathrm{b}, \mathrm{c}, \mathrm{d})=\mathrm{a}^{\prime} \mathrm{bc}{ }^{\prime} \mathrm{d}+\mathrm{ab}^{\prime} \mathrm{cd}$ ', assuming that $\mathbf{a}$ and $\mathbf{b}$ can never both be 1 at the same time and that $\mathbf{c}$ and $\mathbf{d}$ can never both be 1 at the same time
8. Differentiate between Latency and Throughput with examples.

## PART B

(Answer one full question from each module, each question carries 6 marks)

## MODULE I

9. A synchronous sequential machine has a single control input $x$ and the clock and two outputs $A$ and $B$. On consecutive rising edges of the clock, the code on $A$ and $B$ changes from 00 to 01 to 10 to 11 and repeats itself if $x=1$; if at any time $x=0$, it holds to the present state. Draw the state diagram and implement the circuit using T flip-flops.

## OR

10. A museum has three rooms, each with a motion sensor ( $\mathrm{m} 0, \mathrm{~m} 1$, and m 2 ) that outputs 1 when motion is detected. At night, the only person in the museum is one security guard who walks from room to room. Create a circuit that sounds an alarm (by setting an output A to 1) if motion is ever detected in more than one room at a time (i.e., in two or three rooms), meaning there must be one or more intruders in the museum.

MODULE II
11. Explain with appropriate figures, static and dynamic hazards.
12. Draw an ASM chart and state diagram to describe a sequence detector that detects an overlapping sequence of 101 .

MODULE III
13. Use magnitude comparators and logic to design a circuit that outputs 1 when an 8-bit input ' $a$ ' is in between 75 and 100 (both numbers inclusive). Also write an HDL code for the circuit.

## OR

14. Design a 4 bit up/down counter that has four control inputs cnt_up enables counting up, cnt_down enables counting down, clear synchronously resets the counter to all 0 s, and set synchronously sets the counter to all 1 s . If two or more control inputs are 1 , the counter retains its current count value. Use a parallel -load register as building block.

MODULE IV
15. Illustrate micro programmed controller with neat diagram.

## OR

16. Design a 4-bit up-counter with input cnt (1 means count up), clear input clr, a terminal coun output tc, and a 4-bit output Q indicating the present count. After deriving the controller's FSM, implement the controller as a state register and combinational logic.

MODULE V
17. Using the five-step controller design process, design and draw the final implementation of a soda machine dispenser controller. The soda dispenser has three inputs, $\mathbf{c}, \mathbf{s}$, and $\mathbf{a}$. The 8 -bit input $\mathbf{s}$ represents the cost of each bottle of soda. The 1-bit input $\mathbf{c}$ is 1 for one clock cycle when a coin is inserted. The output $\mathbf{d}$ becomes 1 when the soda should be dispensed i.e. when the value of coins inserted into the soda dispenser is greater than or equal to $\mathbf{s}$. The soda dispenser does not give change.

## OR

18. Design a coffee vending machine using RTL Design method.

## MODULE VI

19. Design a 4 bit by 4-bit sequential multiplier and draw an FSM describing the controller behavior of the multiplier. Compute its total gate delay and size

OR
20. Design a 16 bit carry-select adder suing 4-bit ripple carry adders. Compute the size and delay of the circuit.

