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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2017

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

			Marks
1	a)	Convert 326.875_{10} to binary, and Hex form.	(3)
	b)	Represent 478_{10} in BCD and Excess-3 codes.	(3)
	c)	Perform the arithmetic operation on these unsigned binary numbers. Show intermediate steps. i) 10110.101+101.11 (ii) 100001-1011	(4)
	d)	Simplify using K-map F(a,b,c,d) = ∑m (4,5,7,8,9,11,12,13,15)	(5)
2	a)	A function is defined as F(a,b,c,d) = a'b+a'c+c'+a'd+a'b'c'+a'bc' i) Express the function in standard SOP (canonical) form. ii) Implement the function using single 8:1 MUX. iii) Simplify the function using K-map and implement the result using NAND gates only.	(10)
	b)	Design a logic circuit that produces a HIGH output whenever a 3-bit binary number $A_2A_1A_0$ greater than 001 and less than 110 is applied as input (A_2 is MSB).	(5)
3	a)	A computer system uses 12 bits. What is the counting range of values, in decimal form, if the 12 bits are used to represent i) unsigned numbers only (ii) 2's complement system (iii) 1's complement system.	(5)
	b)	Perform arithmetic operation on the given decimal numbers using 2's complement system. Use 8 bits for each number including sign bit. Express the result in binary form. : 15 - 4	(4)
	c)	Design the circuit of a 3-line to 8-line decoder using basic gates.	(6)

PART B

Answer any two full questions, each carries 15 marks.

4	a)	Draw the circuit diagram of a standard 2 input CMOS NOR gate with 5V supply voltage. How does it work as a NOR gate. Write its truth table.	(5)
	b)	What are noise immunity and noise margin? Indicate the logic levels of the 5V CMOS and TTL gates.	(5)
	c)	What is open-collector output gate? State its use. What is tri-state logic? State its use.	(5)
5	a)	Design the circuit of a mod-12 asynchronous up counter using JK flip-flop that starts counting at 0. Draw its output waveforms and indicate the sequence. Design an additional circuit to light an LED when the count is maximum.	(10)
	b)	Consider a 5 bit asynchronousup counter using JK flip-flop. Find its modulus. What is the lowest output frequency, if the input clock frequency is 160 kHz? What is the counting range?	(5)
6	a)	Design a 3-bit synchronous up counter using T Flip-flop with outputs $Q_2Q_1Q_0$ where Q_0 is LSB. Write the complete truth table and excitation table. Derive the expression of T_2, T_1, T_0 in terms of Q_2, Q_1, Q_0. Draw the circuit diagram.	(10)
	b)	What is PLA?Showhowf1= a'bc+ab'+abc', f2= a'b'c'+ac and f3= ab'c+ab can be	(5)

implemented in PLA.

PART C

Answer any two full questions, each carries 20 marks.

7 a) Draw the state diagrams of JK flip-flop. Write its state table. (5)

b) Design the logic circuit using JK flip-flop for the given state table where x is the input. Draw the state diagram, transition table, JK flip-flop excitation table, logic diagrams. (15)

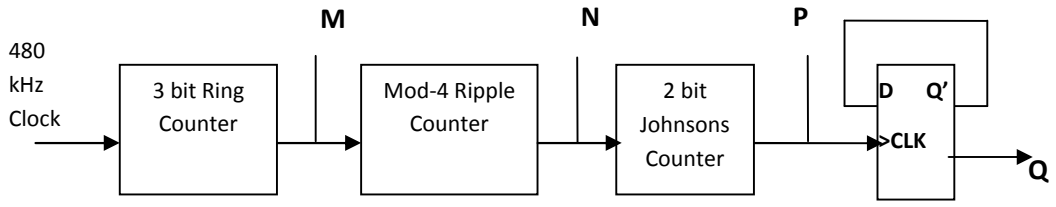
Present state	Next state		Output	
	x=0	x=1	x=0	x=1
A	B	A	0	0
B	B	C	0	0
C	D	A	0	1
D	B	C	0	1

8 a) Find the equivalent states and reduce the given state table using implication chart. x is the input (10)

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	e	c	0	0
b	c	a	0	0
c	b	g	0	0
d	g	a	0	0
e	f	b	1	0
f	e	d	0	0
g	d	g	0	0

b) Design a 3-bit up/down synchronous counter using JK Flip-flop that counts up when the control input M=1 and counts down when M=0. Assume that JK flip-flop inputs are $J2K_2$, $J_1 K_1$,$J_0 K_0$ and the corresponding outputs are Q_2 Q_1 Q_0 respectively where Q_0 is LSB. Draw its State table, Excitation Table and Logic diagram (10)

9 a) A logic circuit is designed using the following modules. First module is a 3-bit ring counter. A clock signal of 480 kHz is applied at the clock input of this module. The output from its last FF is M. This output is connected to the clock input of the next stage which is a mod-4 ripple counter. The output from its last flip-flop is N. This output is connected to the clock input of the 2-bit Johnsons counter. The output P of its last Flip-flop is applied to the clock input of an edge triggered D flip-flop. The Q' of the D flip-flop is connected to the D input. Find the frequency of the output signals at M, N, P and Q. Justify your answer. What is the overall modulus? (10)



b) Design a 4-bit bi-directional shift register circuit using D flip-flops with shift control input M that shifts right when M=1 and shifts left when M=0. State how it works with examples. (10)

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