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| **Scheme of Valuation/Answer Key**  (Scheme of evaluation (marks in brackets) and answers of problems/key) | | | | | |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  FIFTH SEMESTER B.TECH (S) DEGREE EXAMINATION, MAY 2019 | | | | | |
| **Course Code: CS305** | | | | | |
| **Course Name: MICROPROCESSORS AND MICROCONTROLLERS** | | | | | |
| Max. Marks: 100 | | |  | Duration: 3 Hours | |
| **PART A** | | | | | |
|  |  | ***Answer all questions, each carries 3 marks.*** | | | Marks |
| 1 |  | Draw the timing diagram for the 8086 minimum mode memory write operation.  **Scheme**:  Timing diagram – 3 marks. Maximum 3 marks | | | (3) |
| 2 |  | With an example describe the register and register relative addressing mode of 8086.  **Scheme**:  Definition of register addressing mode with explanation – 1.5 marks  Definition of register relative addressing mode with explanation – 1.5 marks | | | (3) |
| 3 |  | List any six features of the 8088 processor.  **Scheme**:  Any six features 0.5 marks for each feature. Maximum 3 marks | | | (3) |
| 4 |  | Describe the usage of the 8086 instructions: PUSH, POP and PUSHF  **Scheme**:  Each instruction with correct explanation – 1 mark. Maximum 3 marks | | | (3) |
| **PART B** | | | | | |
| ***Answer any two full questions, each carries 9 marks.*** | | | | | |
| 5 | a) | With a neat diagram describe how 8086 memory is organised at physical level.  **Scheme**:  Diagram – 2 marks, Explanation– 2 marks. Maximum 4 marks | | | (4) |
|  | b) | With the help of an example show how stack can be used for passing parameters to a subroutine in assembly programs.  **Scheme**:  Basic explanation – 3 marks, example – 2 marks. Maximum 5 marks | | | (5) |
| 6 | a) | Write an 8086 assembly program to find the largest number from a list of numbers.  **Scheme**:  Program Logic – 4 marks, Program structure – 3 marks, correctness of the logic – 2 marks. Maximum 9 marks | | | (9) |
| 7 | a) | What are assembler directives? List any four assembler directives and its usage.  **Scheme**:  Assembler directive definition – 1 marks, any four assembler directives – 4 marks. Maximum 5 marks | | | (5) |
|  | b) | What are the different information conveyed by the Queue status signals QS0 and QS1 of 8086 in maximum mode?  **Scheme**:  Meaning corresponding to the different bit combination – 1 mark each Maximum 4 marks. | | | (4) |
| **PART C** | | | | | |
| ***Answer all questions, each carries 3 marks.*** | | | | | |
| 8 |  | What are the basic categories of 8086 software interrupts?  **Scheme**:  Dedicated, reserved and user defined. Proper explanation. Maximum 3 marks | | | (3) |
| 9 |  | Describe the control word format for the BSR mode of 8255.  **Scheme**:  Control word format with proper explanation of each bits. Maximum 3 marks | | | (3) |
| 10 |  | What is an Interrupt Service Routine? How do we get the address of the ISR corresponding to a given interrupt in 8086?  **Scheme**:  Definition of ISR – 1 marks. Mentioning of vector table to retrieve ISR address – 2 marks. Maximum 3 marks | | | (3) |
| 11 |  | What are the purposes of the signals DRQ, TC and MARK in 8257?  **Scheme**:  Proper explanation for each signal. Maximum 3 marks. | | | (3) |
| **PART D** | | | | | |
| ***Answer any two full questions, each carries 9 marks.*** | | | | | |
| 12 |  | With a neat diagram describe how 8259 can be used for handling multiple interrupts?  **Scheme**:  Diagram – 4 marks, Proper explanation of the concept—5 marks.  Maximum 9 marks | | | (9) |
| 13 |  | With a neat diagram describe the architecture of 8255.  **Scheme**:  Diagram – 3 marks, Explanation of function units – 4 marks, Overall description of the functioning – 2 marks. Maximum 9 marks. | | | (9) |
| 14 | a) | What are the different input modes of 8279?  **Scheme**:  Description of each modes. Maximum 5 marks | | | (5) |
|  | b) | Describe the sequence of steps for developing and deploying an ISR for handling interrupt in 8086.  **Scheme**:  Maximum 4 marks | | | (4) |
| **PART E** | | | | | |
| ***Answer any four full questions, each carries 10 marks.*** | | | | | |
| 15 | a) | Describe different types of microcontrollers.  **Scheme**:  Explanation of different types -5 marks | | |  |
| b) | What are the different criteria that should be considered while selecting a microcontroller?  **Scheme**:  Explanation of different criteria - 5 marks | | | (10) |
| 16 | a) | What are the different operating modes of 8253?  **Scheme**:  Proper explanation for each mode. Maximum 6 marks | | | (6) |
|  | b) | Describe any four control transfer instructions of 8051?  **Scheme**:  1 mark for each instruction. Maximum 4 marks. | | | (4) |
| 17 | a) | What are the Special Purpose Registers of 8051?  **Scheme**:  Description of each registers. Maximum 4 marks | | | (4) |
|  | b) | What is the structure of the Program Status Word(PSW) of 8051?  **Scheme**:  Explanation of various bits- 3 marks Maximum 3 marks. | | | (3) |
|  | c) | How the stack operations of 8051 differ from 8086?  **Scheme**:  Explanation of stack operations- 3 marks | | | (3) |
| 18 |  | Write an 8051 program to count the number of 1s in the binary representation of a given number.  **Scheme**:  Program Logic – 4 marks, Program structure – 4 marks, correctness of the logic – 2 marks. Maximum 10 marks | | | (10) |
| 19 |  | Explain the internal memory organization of 8051.  **Scheme**:  Explanation – 10 marks Maximum 10 marks | | | (10) |
| 20 | a) | Explain any five addressing modes of 8051 with example  **Scheme**:  1 mark for each addressing mode. Maximum 5 marks | | | (5) |
|  | b) | What is the use of following 8051 instructions: ADDC, SUBB, CPL, RLC and SWAP?  **Scheme**:  1 marks for each instruction. Maximum 5 marks | | | (5) |
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