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| **Scheme of Valuation/Answer Key**  (Scheme of evaluation (marks in brackets) and answers of problems/key) | | | | | |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  V SEMESTER B.TECH (S) EXAMINATION, DECEMBER 2018MAY 2019 | | | | | |
| **Course Code: AE305** | | | | | |
| **Course Name: MICROPROCESSORS & MICROCONTROLLERS** | | | | | |
| Max. Marks: 100 | | |  | Duration: 3 Hours | |
|  | | | | | |
| **PART A** | | | | | |
|  |  | ***Answer any two full questions, each carries 15 marks.*** | | | Marks |
| 1 | a) | Diagram 4 marks, explanation 3marks | | | (7 ) |
|  | b) | Procedure explanation 1mark, 4 differences – 1 marks each | | | (5) |
|  | c) | Interrupt definition- 1 marks, ISR execution- 2 marks | | | (3) |
| 2 | a) | Assembly process flow chart - 4 marks  Editor,assembler,linker,loader,debugger-4 marks | | | (8) |
|  | b) | Each instruction 1 mark | | | (4) |
|  | c) | Listing of flag bits and its use | | | (3) |
| 3 | a) | Diagram 3, Explanation 4 | | | (7) |
|  | b) | Assembler directive explanation – 1 mark  Each assembler directive- 1 mark (total-4 marks) | | | (5) |
|  | c) | Stack operation – 1 mark  Example -2 marks | | | (3) |
| **PART B** | | | | | |
| ***Answer any two full questions, each carries 15 marks.*** | | | | | |
| 4 | a) | Architecture – 4 marks  Various blocks explanation- 4 marks | | | (8 ) |
|  | b) | Explanation 3 marks | | | (3) |
|  | c) | Circuit with signal names 4marks | | | (4) |
| 5 | a) | Interfacing circuit- 3 marks  Procedure- 4marks | | | (7) |
|  | b) | Descriptor format -3 marks  Explanation-2 marks | | | (5) |
|  | c) | Pentium special features – 3 marks | | | (3) |
| 6 | a) | Branch prediction 4marks, explanation with example 4marks | | | (8) |
|  | b) | Architecture 4marks | | | (5) |
|  | c) | Functions of signals 1mark each | | | (2) |
| **PART C** | | | | | |
| ***Answer any two full questions, each carries20 marks.*** | | | | | |
| 7 | a) | Different addressing modes 2marks, 2 examples in each mode with explanation 8marks | | | (10) |
|  | b) | 3 differences 1 mark each (1x3=3) | | | (3) |
|  | c) | Program – 7 marks, partial credit may be given for correct logic/algorithm | | | ( 7) |
| 8 | a) | 1 mark each 1x3 | | | (3) |
|  | b) | PSW Format- 2 marks  Explanation -3 marks | | | (5) |
|  | c) | Circuit- 4 marks  Program - 8 marks | | | (12) |
| 9 | a) | Any 10 registers -1 Mark each | | | (10) |
|  | b) | Interfacing circuit-3 marks | | | (3) |
|  | c) | Program 7 marks, partial credit may be given for correct logic/algorithm | | | (7) |
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