

Scheme of Valuation/Answer

(Scheme of evaluation (marks in brackets) and answers of problems/key)

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: EE309

		Course Name: MICROPROCESSOR AND EMBEDDED SYSTEMS	
Ma	x. M	arks: 100 Duration: 3	Hours
		PART A	Marks
		Answer all questions, each carries5 marks.	
1		A=D5 _H (2.5 marks), CY=0,AC=1,P=0,Z=0,S=0(2.5marks)	(5)
2		Program (2.5 marks), Max. delay=1.1ms (2.5 marks)	(5)
3		Mode 0, mode1, mode2 operation explanation (5 marks)	(5)
4		Assembler (2.5 marks), Compiler (2.5 marks),	(5)
5		List any two bit handling instruction and explain its operation (5 marks)	(5)
6		Eg:-SETB bit, CLR bit Addressing modes with eg:- (5 marks)	(5)
-			(5)
7		Program (5 marks)	(5)
		Students making a positive attempt to answer this question may be provided	
		with proportional weightag <mark>e of ma</mark> rks.	
8		Explain- ORG, EQU, END (5 marks)	(5)
	1	PART B	
		Answer any twofull questions, each carries10 marks.	
9		Programs with comments (10 marks)	(10)
		Students making a positive attempt to answer this question may be provided	
		with proportional weightage of marks.	
10	a)	Explain machine cycle(3), T state (2)	(5)
	b)	Explain CALL and RET (5marks)	(5)
11	a)	Draw timing digOF+MR+MW (6 marks)	(6)
	b)	MOV A,M(2 marks), XCHG (2 marks)	(4)
	I	PART C	I
		Answer any twofull questions, each carries10 marks.	



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12	a)	Memory allocation table(4 marks), Memory interface circuit(6 marks)	(10)
13		Explain(10 marks)	(10)
14	a)	Interrupt structure (6 marks)	(6)
	b)	List 4 difference(4 marks)	(4)
		PART D	
		Answer any twofull questions, each carries 10 marks.	
15		Diagram(5 marks), Explain(5 marks)	(10)
16		Program (10 marks)	(10)
		Students making a positive attempt to answer this question may be provided	
		Students making a positive attempt to answer this question may be provided with proportional weightage of marks.	
17	a)		(4)
17	a)	with proportional weightage of marks.	
17	a) b)	<i>with proportional weightage of marks.</i> 2 bit jump instruction (2 marks)	
17	,	 <i>with proportional weightage of marks.</i> 2 bit jump instruction (2 marks) 2 byte jump instruction (2 marks) 	(4)

