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| **Scheme of Valuation/Answer Key**(Scheme of evaluation (marks in brackets) and answers of problems/key) |
| **APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**FIFTH SEMESTER B.TECH DEGREE EXAMINATION, JULY 2019 |
| **Course Code: EC361** |
| **Course Name: DIGITAL SYSTEM DESIGN** |
| Max. Marks: 100 |  | Duration: 3 Hours |
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| **PART A**  |
|  |  | ***Answer any two full questions, each carries 15 marks.*** | Marks |
| 1 | a) | Sample sequence - 1State diagram – 1state table - 1transition table – 1excitation table – 1expressions for output and excitation – 1circuit diagram –2 | (8)  |
|  | b) | Difference – 2ASM chart – 4number of ASM blocks - 1 | (7) |
| 2 | a) | Timing diagram with states – 1Flow table – 1.5Flow diagram – 1.5Transition table –1Expression –1circuit diagram –2 | (8) |
|  | b) | expressions for output and excitation – 1Mealy / Moore - 1excitation table – 1.5transition table – 1.5state table - 1State diagram – 1 | (7) |
| 3 | a) | expressions for output and excitation – 1Mealy / Moore - 1excitation table – 1.5transition table – 1.5state table - 1State diagram – 1 | (7) |
|  | b) | assumptions – 1.5state diagram – 1.5state table – 1excitation table – 2ckt diagram – 2 | (8) |
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| **PART B**  |
| ***Answer any two full questions, each carries 15 marks.*** |
| 4 | a) | static (1 and 0) - 1dynamic (1 and 0)–1examples - 2.5 + 2.5 | (7) |
|  | b) | contact bounce and explanation with waveform and circuit– 1 + 1 + 1debounce ckt + waveform+ explanation–1.5 + 1.5 + 1sr latch – 1 | (8) |
| 5 | a) | path selection – 1 + 1test vector generation for the path – 3 + 3 | (8) |
|  | b) | logic diag – 1df/da and df/dd – 2.5 + 2.5test vector – 1 + 1 | (7) |
| 6 | a) | circuit diag – 1table for faulty and fault free outputs –3fault cover table –2ETV -1STV -1 | (8) |
|  | b) | Deterministic TG – 3.5Semirandom TG- 3.5 | (7) |
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| **PART C**  |
| ***Answer any two full questions, each carries 20 marks.*** |
| 7 | a) | PLA diagram – 2PLa program array table – 2SSR notation – 2SSR specification – 2compatibility matrix - 2 | (10) |
|  | b) |  | (10) |
| 8 | a) | 1 + 3 + 4 | (8) |
|  | b) | Diagram – 6Explanation - 6 | (12) |
| 9 | a) | Diagram – 5Explanation - 5 | (10) |
|  | b) | PLA diagram – 2PLa program array table – 2SSR notation – 2SSR specification – 2compatibility matrix - 2 | (10) |
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